Bottom-Gate TFTs with Channel Layer Grown by Pulsed PECVD Technique

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ABSTRACT

In this paper, we report on nc-Si:H thin films deposited by the pulsed PECVD technique at a temperature of 150°C and TFTs made using this material. RF power and silane flow rate were varied in order to study the effect of different levels of crystallinity on the film. Electrical conductivity, Hall mobility, optical transmittance, and Raman backscattering were measured on films of two different thicknesses. From the Raman data we see that the 50 nm films with hydrogen dilution are mostly amorphous, indicating the presence of a thick incubation layer. The values obtained for the conductivity, mobility, and optical gap varied depending on the processing conditions and these results are discussed. Bottom-gate TFTs were fabricated using a pulsed PECVD channel layer and a SiN gate dielectric. The TFTs' extracted parameters are $\mu_{sat} \leq 0.38 \text{ cm}^2/(\text{V} \cdot \text{s})$, $V_{t,sat} \geq 7.3 \text{ V}$, $I_{on/off} > 10^6$, and $S < 1 \text{ V/decade}$. The TFT performance and material properties are presented and discussed.

INTRODUCTION

Hydrogenated amorphous silicon (a-Si) is used in thin-film transistors (TFTs) for flat-panel displays (FPD) and large-area imagers, and it is also a promising photovoltaic material. a-Si TFTs have a low off-current and sufficient on-current for most applications; however, they suffer from poor carrier mobility and threshold voltage (V_t) shift. Its low mobility (μ) places a limitation on pixel sizes for display and imaging applications, and its poor hole mobility prohibits a usable p-type device. Its drifting threshold voltage also means that it cannot be used easily or reliably in column multiplexer and row shift register circuits [1]. Polycrystalline silicon can overcome the disadvantages of a-Si TFTs; however, it has some drawbacks, with regards to cost and reliability.

Alternatively, nanocrystalline silicon (nc-Si:H) is deposited by plasma-enhanced chemical vapour deposition (PECVD) and can thus be easily integrated into standard PECVD systems with little additional cost. In theory, it can provide equal or increased mobility and improved stability over its amorphous counterpart due to its crystallinity; however, in practice this is not always the case [1]. Recently, nc-Si:H films deposited by pulsed PECVD for use in solar cells have been reported [2]. Pulsed PECVD is the same as conventional PECVD at 13.56 MHz, except the plasma is modulated with a frequency in the kHz range. During the off-cycles, negatively charged particles can be neutralized, thus reducing the density of powder particles [3]. This allows the growth rate to be increased without compromising the material's quality. Because of these advantages and its success so far as a solar cell material, pulsed PECVD may be a promising deposition technique for the channel layer of nc-Si:H TFTs.

In this paper, the experimental results from the electrical (conductivity, mobility), optical (energy band gap), and structural (crystallinity) characterizations of the films grown by pulsed PECVD are presented and discussed, along with the characteristics and extracted parameters of bottom-gate TFTs made with a pulsed PECVD-grown active layer.

EXPERIMENT

A series of four silicon thin films were deposited at 150 °C with different processing conditions, which are summarized in Table I. The films were deposited by pulsed PECVD, a

Table I. Film deposition parameters

Film	SiH ₄ Flow Rate	H ₂ Flow Rate	Power	Pressure
1 (a-Si)	20 sccm	0 sccm	2 W	0.4 Torr
2, 3, 4 (nc-Si)	2 – 4 sccm	100 sccm	40 – 100 W	1.8 Torr

standard 13.56 MHz PECVD process, but modulated in the 1 to 100 kHz range with a duty cycle of 10-50 %. For all films, the plasma pulsing frequency was kept constant at 60 kHz. Film 1 is deposited with no hydrogen dilution and low RF power and is thus amorphous. For films 2, 3, and 4, the SiH₄ flow rate and RF power were varied, in order to produce differing degrees of (220) or (111) grain orientation in the crystallites [2]. The 50 nm films are labelled 50-1, 50-2, 50-3, 50-4, and the 300 nm films are labelled 300-1, 300-2, 300-3, 300-4, where the suffix denotes the process conditions used.

Material characterization was done using films grown on Corning 1737 glass with a thin (30 nm) SiN cap to prevent any contamination and post-oxidation. This cap was etched in BHF prior to any material or electrical characterization. The conductivity of the samples was measured using co-planar electrodes (spacing of 1.3 mm long and 10 mm wide) of silver paste and applying a voltage sweep from 0-20 V while measuring the current. The Hall effect mobility was measured using a method similar to that described in [4] at 25 °C in a magnetic field of ≈ 0.43 T. A square sample (1 cm $\times$ 1 cm) with small ohmic Aluminium contacts deposited on each corner by electron-beam evaporation was used. The change in the Hall voltage was measured as the magnetic field was reversed multiple times. The optical band gap was measured using a Shimadzu UV spectrometer, and Raman measurements were done using a 632.5 nm wavelength He-Ne laser.

We fabricated bottom-gate TFTs using a standard top-passivated, wet-etch process. A 250 nm silicon nitride (SiN) gate dielectric was deposited at a substrate temperature of 250 °C on top of a 120 nm molybdenum gate pattern. Next, a 50 nm active Si channel layer of was deposited at 150 °C by pulsed PECVD, followed by a top SiN layer at 150 °C to complete the tri-layer. After opening the source and drain contacts, a n⁺ μ c-Si:H / SiN bilayer was deposited at 150 °C by PECVD, followed by a final Al metallization layer. Prior to characterization, the TFT wafers were annealed at 150 °C for 2 hours to improve the contact properties. The TFTs have gate lengths (L) ranging from 25 μ m to 200 μ m, and the channel width (W) is a constant 100 μ m. The TFTs are labelled TFT-1, TFT-2, TFT-3, TFT-4, where the suffix denotes the corresponding process condition. The TFTs were characterized using a Keithley SCS-4200 system.

Figure 1. Raman measurements of (a) 50 nm films and (b) 300 nm films

RESULTS

Material properties

For each of the four sets of process conditions, a 50 nm thick sample (which is the same as the channel layer of the TFT) and a 300 nm thick sample were used for material characterization, the results of which are summarized below:

The Raman data is shown in Figures 1(a) and (b). The crystallinity was calculated from $X_c = (I_{500} + I_{520}) / (I_{500} + I_{520} + 0.8I_{480})$, where I_n denotes the area of the fit Gaussian peak at wavenumber n [5]. The 400 - 550 cm^{-1} range was used for the fitting. Attempting to extract the crystalline fraction from the 50 nm film data in Figure 1(a) does not yield any useful result as the films appear to be amorphous. The crystallinity is high in samples 300-3 and 300-4 (60 % and 75 % respectively), and negligible in 300-2 (10 %).

The dark conductivity (σ_{dark}) and photo conductivity (σ_{photo}) are plotted in Figure 2. All of the 50 nm samples show a σ_{dark} on the order of $10^{-9} (\Omega \cdot \text{cm})^{-1}$; however, samples 50-3 and 50-4 show a slightly higher σ_{dark} and a reduced σ_{photo} compared to 50-1. Film 300-1 accordingly shows a low σ_{dark} and high σ_{photo} , typical a-Si films. Film 300-2 shows similar values even though hydrogen dilution was high during this deposition and there was some crystalline fraction present, according to Figure 1(b). 300-3 and 300-4 show a high σ_{dark} ($\approx 10^{-5} - 10^{-3} (\Omega \cdot \text{cm})^{-1}$) and a small $\sigma_{\text{photo}} / \sigma_{\text{dark}}$ which is expected for these high crystallinity films [6].

Hall effect measurements were also performed to further investigate the electrical properties of the highly crystalline films. Figure 3 shows the Hall voltage obtained while a voltage of 100 V was applied to sample 300-4. The average Hall voltage was 1.15 mV, yielding a calculated carrier concentration of $n = 1.1 \times 10^{17} \text{ cm}^{-3}$ and a mobility of approximately $0.27 \text{ cm}^2 / (\text{V} \cdot \text{s})$.

The optical band gap, estimated by a linear fit to a Tauc plot is show in Figure 4. The 50 nm samples show a slight upward trend. The bandgap of the 300 nm films increases with increasing film crystallinity and shows an overall higher band gap compared to the 50 nm films.

Figure 2. Dark (σ_{dark}) and photo (σ_{photo}) conductivity for all samples. The short horizontal lines are error bars.

Figure 3. Hall voltage (V_H) of sample 300-4 over time as the magnetic field was reversed at the points indicated by the arrows.

TFT characteristics

To study the usefulness of a TFT channel layer grown by pulsed PECVD, we fabricated bottom-gate TFTs. The thickness of the channel was 50 nm to reduce leakage current and light-induced effects. The transfer and output characteristics of one TFT from sample TFT-3 are shown in Figures 5(a) and 5(b) respectively, along with the extracted values for this particular TFT. Values for linear and saturated mobility (μ_{lin} and μ_{sat}) and linear and saturated threshold voltage ($V_{t,lin}$ and $V_{t,sat}$) were extracted using a simple equation for the drain current in the linear regime and saturation regime as described in [7]. From the transfer characteristics with $V_{DS} = 10$ V, the off-current (I_{off}) and on-current (I_{on}) are defined as the minimum and maximum current respectively. The on-off ratio ($I_{on/off}$) is given by $I_{on} \div I_{off}$ and the subthreshold slope (S) is defined as the inverse maximum slope. The extracted TFT parameters are summarized in Table II. All of the TFTs show a high V_t and S . TFT-3 and TFT-4 display better threshold voltage and field-effect mobility compared to TFT-2; however, TFT-2 shows slightly improved sub-threshold slope and extremely low leakage ($I_{off} < 10^{-14}$). The values of μ_{sat} for TFT-4 are similar to the mobility measured by the Hall effect ($0.27 \text{ cm}^2 / (\text{V} \cdot \text{s})$). The gate leakage (I_G) was consistently $\approx 10^{-13} - 10^{-12}$ A for all TFTs.

The stability of the TFT was measured by stressing the TFT with $V_G = 30$ V and $V_D = V_S = 0$ V, then measuring the linear ($V_{DS} = 0.1$ V) and saturation ($V_{DS} = V_G$) transfer characteristics either every five minutes for up to 30 minutes or every 60 minutes for up to 2 hours. Figure 6 shows the change in the threshold voltage over time, beginning with the first measurement, which was done before any stress was applied. The V_t shift in these TFTs is very high, and after two hours still no saturation is observed.

Figure 4. Optical band gap data

Figure 5. (a) Transfer characteristics and (b) output characteristics for TFT-3, die I5

Table II. Extracted parameters for TFTs with $L = 25, 50, 75, 100, 200 \mu\text{m}$ and $W = 100 \mu\text{m}$

TFT	$\mu_{lin} \left(\frac{\text{cm}^2}{\text{V}\cdot\text{s}} \right)$	$\mu_{sat} \left(\frac{\text{cm}^2}{\text{V}\cdot\text{s}} \right)$	$V_{t,lin} \text{ (V)}$	$V_{t,sat} \text{ (V)}$	$S \left(\frac{\text{V}}{\text{decade}} \right)$	$I_{on/off}$	$I_{off} \text{ (A)}$
TFT-2	0.02-0.10	0.12-0.17	9.9-12.4	11.6-13.6	0.46-0.81	$> 10^7$	$< 10^{-14}$
TFT-3	0.23-0.27	0.34-0.38	9.6-11.3	7.5-9.6	0.76-0.95	$> 10^6$	$< 10^{-12}$
TFT-4	0.28-0.30	0.34-0.46	11.8-13.0	7.3-9.5	0.76-1.20	$> 10^6$	$\leq 10^{-12}$

DISCUSSION

The 50 nm samples appear mostly amorphous according to the Raman data of Figure 1(a); however, one can see that the peak widths of the 50-2, 3, and 4 samples are much less than that of 50-1 indicating a different material structure. The reduced σ_{photo} and increased σ_{dark} of 50-3 and 50-4 in Figure 2, and the increased band gap in Figure 4 indicates that the 50-3 and 50-4 films may contain fine crystallites embedded in an amorphous matrix [8]. The crystallinity of the 50 nm layers was not high as expected based on previous data from Das et. al. [3, see Figure 5]. Crystalline growth is affected by the substrate [3], and in the case of these bottom-gate TFTs the active layer was deposited on top of an SiN layer which delayed the onset of crystal growth. As the films grew thicker, the crystallinity increased as well as the conductivity, as seen in samples 300-3 and 300-4. Samples 50-3 and 50-4 are thus incubation layers for crystalline growth. The value for the free carrier concentration obtained from Hall effect measurements of sample 300-4 is much higher than that of intrinsic silicon ($\sim 10^{10} \text{ cm}^{-3}$), and therefore we conclude that the high σ_{dark} in 300-3 and 300-4 is mostly due to oxygen contamination in the film, which is known

Figure 6. Threshold voltage shift measured every 5 minutes and every 60 minutes for six different TFTs

to act as a donor along the grain boundaries of nc-Si:H [9].

The electrical performance of the TFTs (see Table II) is comparable to previous pulsed PECVD TFT work [10] and other low temperature a-Si TFTs [11]. The mobility, off-current, and on-off ratio are more than acceptable for pixel switching applications; however, the threshold voltage (V_t) and sub-threshold slope (S) are both high, which is most likely due to the low temperature channel layer being defective or a defective SiN/channel interface due to an unoptimized bottom SiN gate dielectric. The high threshold voltage shift of the TFT seen in Figure 6 supports both these claims as it is widely known that V_t shift is related to defects at the SiN/channel interface and/or SiN bulk. The performance of these TFTs could be improved by reducing the incubation layer thickness and the improving the quality of the SiN layer.

CONCLUSIONS

Individual 300 nm films show a high crystallinity, while 50 nm films are mostly made up of an amorphous incubation layer. The TFTs showed the following characteristics: $\mu_{sat} < 0.38 \text{ cm}^2/(\text{V} \cdot \text{s})$, $V_{t,sat} \geq 7.3 \text{ V}$, $I_{on/off} \geq 10^6$, $S < 1 \text{ V/decade}$, and a high V_t shift under gate bias stress. Pulsed PECVD has demonstrated that it can produce a highly crystalline material. The TFT results are promising and could easily be improved through further optimization of the SiN and channel layers enabling nc-Si:H TFTs on flexible substrates.

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