# Low-Temperature Processing of Polycrystalline Silicon Films using Laser Crystallization

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December 18, 2002

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# 1 Introduction

Amorphous silicon (a-Si) or hydrogenated amorphous silicon (a-Si:H) has been the most commonly used semiconductor for large area applications, most commonly liquid-crystal active-matrix thin-film transistor (TFT) displays, like that shown in Figure 1. More recently,

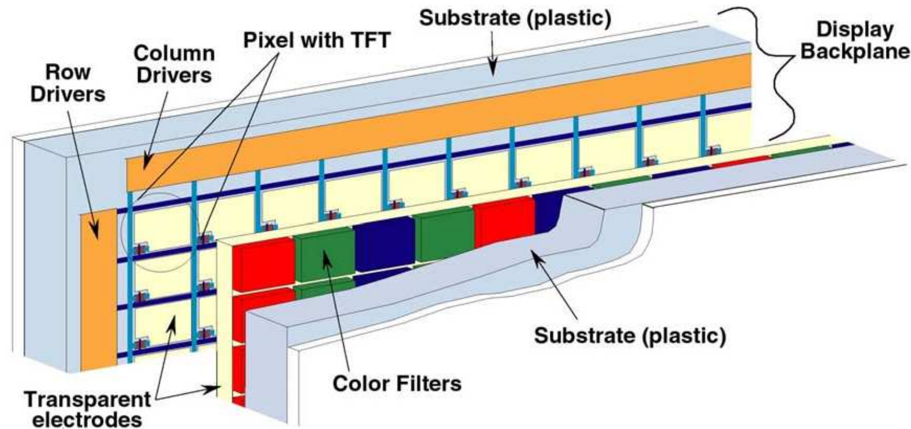


Figure 1: Cut-away view of TFT-LCD, showing backplane with array of TFT pixel switches and integrated driver circuit area. Liquid crystal fills the gap between the backplane and the front plate [1].

TFTs are been used in large-area imaging applications such as X-ray imagers and flat-bed scanners as well. The advantages of a-Si TFTs include good uniformity over large areas, low-leakage current, and the ability to fabricate devices at low temperatures on low melting-point substrates such as glass. Most glass substrates have a softening point in the vicinity of 600$^o$C, however, more recently some glasses such as the Corning Eagle2000 have been fabricated with softening points of 667$^o$C [2]. In general, low temperature substrates will be considered to be those with melting points below 600$^o$C. Using flexible plastic substrates on the other hand, would require a lowering of the maximum processing temperatures to the 120$^o$ - 275$^o$C range [1].

Amorphous silicon can be deposited on low temperature substrates, however, its applications are limited, due to it's low mobility ($\mu_e < 1\ cm^2\ V^{-1}\ s^{-1}$) and it's inability to carry large currents. The a-Si *p*-type doped material has such a low mobility that it forbids the use of complementary logic devices using a-Si. a-Si devices are best used as the switching elements in large-area active pixel arrays (either displays or imagers). Their large bandgap provides little thermal generation of carriers, and thus low "dark" leakage current, which is an important characteristic in active-matrix pixel applications.

Polycrystalline silicon (poly-Si), on the other hand, can have a mobility as high as

100 $cm^2\ V^{-1}\ s^{-1}$ using the more common poly-Si processing techniques, and perhaps higher [1, 3, 4, 5, 6], depending on the processing technology used. As high as 566 $cm^2\ V^{-1}\ s^{-1}$ has been reported by Hara [7]. Brotherton has shown that for an active matrix array of the dimensions of a television (575 × 720), less than 1 $cm^2\ V^{-1}\ s^{-1}$ is required for the row driver TFTs, which is slow enough for a-Si TFTs. Slightly greater than 100 $cm^2\ V^{-1}\ s^{-1}$ is required for the column drivers [8] (see Figure 2). Of course, for much higher resolution displays, greater speed will be required.

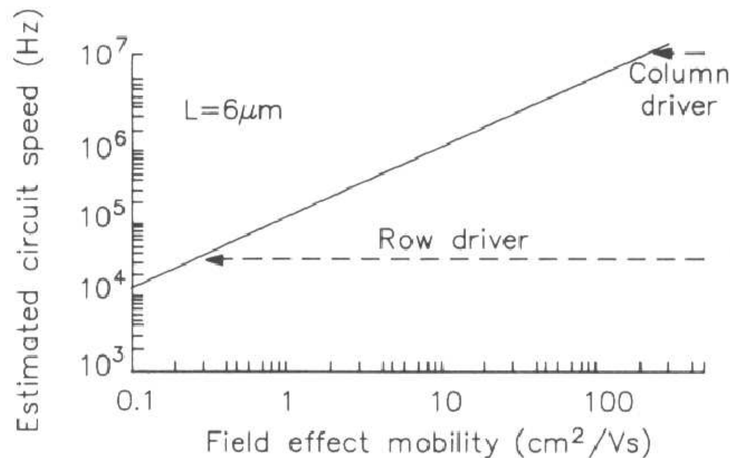


Figure 2: Relationship between circuit speed and mobility for a device with 6 $\mu m$ channel length. From [8].

Poly-Si can be doped $n$-type or $p$-type for use in CMOS circuits and can provide higher current-carrying capability. These advantages make poly-Si a good candidate for the driver circuits (shift registers, multiplexers, and amplifiers) in display/imaging applications, in which integrated circuits made of crystalline silicon as normally used, external to the array itself. This makes for expensive packaging. The main advantage of poly-Si over crystalline silicon is that it can be integrated directly onto the glass panels along with a-Si, thus reducing the demands on packaging and eliminating the need for external driver circuits. The integration of poly-Si devices and a-Si:H TFT active matrix pixels on the same substrate will lead to SoG (System-on-Glass) technology, for highly portable, compact displays and imagers. Figure 3 illustrates how poly-Si can be used to reduce the number of electrical lines connected to the panel which help reduce the external real estate used by crystalline silicon ICs. In this figure, the number of row/gate drivers is reduced to only a gate and clock line, and the number of column drivers is reduced by a factor of four due to multiplexing/demultiplexing. The array could either be an imaging array, or a display.

Polycrystalline silicon is a form of silicon which ideally contains no amorphous phase. It is not formed from a single-crystal, however, so it contains many crystalline areas of

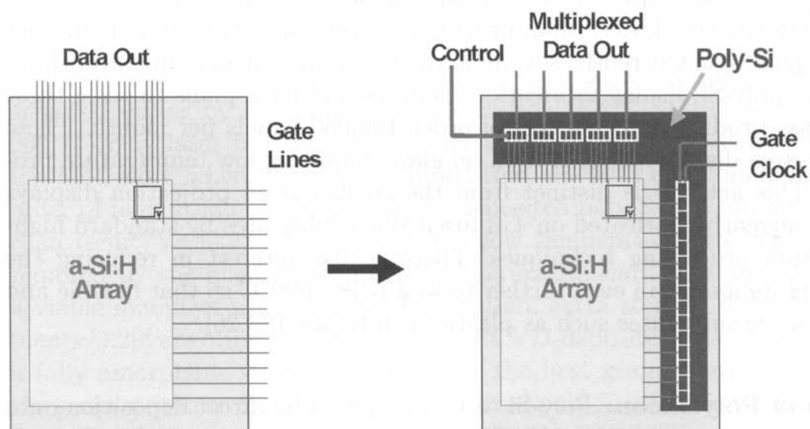


Figure 3: Simplified packaging allowed by poly-Si peripheral circuits on an amorphous Si large-are array [9].

different crystallographic orientation separated by grain boundaries. The areas enclosed by grain boundaries are called grains. Figure 4 shows a polycrystalline silicon sample with many small ($\sim 50-100$ $nm$) grains. These grain boundaries are what limit the performance of

Figure 4: An image of a poly-Si sample taken using a microscope. The grains in the picture are about $\sim 50-100$ $nm$ in diameter.

poly-Si devices, compared to their fully crystalline counterparts.

Producing high quality poly-Si is not without its challenges. Grain boundaries are the main limiting factor in the electrical performance of poly-Si TFTs, so creating larger grain sizes can reduce the areal density of grain boundaries in the material. Having large grains, however, reduces the total number of grains per TFT channel for example, which can translate to less homogeneity across all devices. If some TFT channels have only a few grain

boundaries ($< 3$), and others have more, then the mobility can vary by large percentages across devices. Although having smaller grain sizes can degrade performance, it can also improve homogeneity, by making all devices “equally defective”. This is somewhat analogous to a-Si:H devices, which are uniform across large areas because they are already so defective, that small defects go unnoticed. Grain boundaries also cause large numbers of trapping states to be created, caused by dangling Si bonds. These can be reduced, however, by an extra passivation processing step. Thus, device-grade material can and has been made using laser crystallization and devices with excellent characteristics have been fabricated [9]. Currently the main challenge in creating large area poly-Si devices is in obtaining homogeneity in device parameters. Any variations in grain size, surface topology, interface structures, and the like translate into variations in the device parameters [9].

# 2 Conduction in Poly-Si

As said above, the grain boundaries in poly-Si are what limit the performance in poly-Si devices. Within one grain of material (assuming no defects inside the grain) the electrical transport is essentially the same as that achieved in single-crystal silicon. There are two mechanisms by which grain boundaries limit performance. The first is by introducing changes in the lattice structure which reduce the extent of electron Bloch waves in the material, and cause the electrons to scatter at grain boundaries. The second is by introducing trapping sides at the grain boundary interface, which can trap charge. The latter becomes a significant effect when observing the mobility of doped poly-Si. Figure 5 shows that the mobility is seriously reduced as the number of acceptor impurities is increased. This is not due to

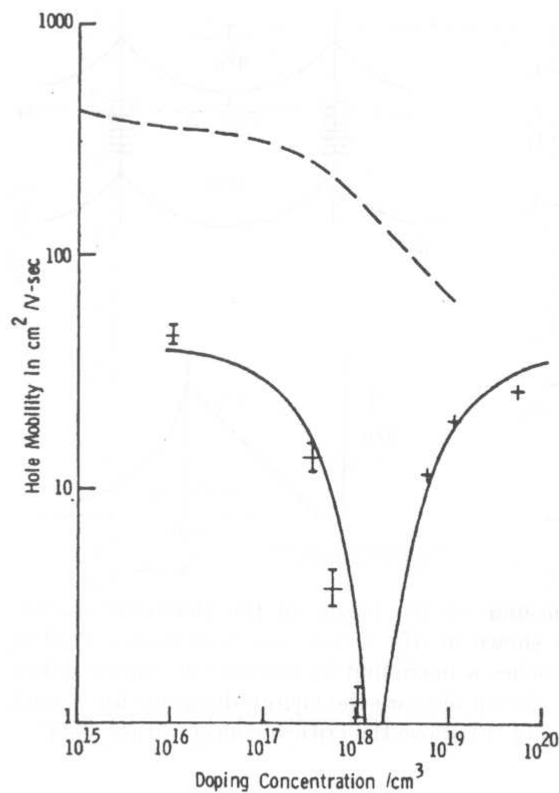


Figure 5: The hole mobility as a function of Boron doping in poly-Si (data points). The solid line is that predicted by a model, and the dashed line is the mobility of crystalline silicon. From [10].

scattering from ionized impurities as in crystalline silicon, however, but due to band bending at the grain boundary interfaces due to an accumulation of carriers there. The charge carriers provided by the dopants fall into the traps, and a depletion of charge from the interior of the grain itself leaves behind space charge. From the charge distribution, the electric field can

be found using Poisson's equation, and from the electric field, the shape of the energy bands can be found. What one finds is that there are barriers at each grain boundary which impede the further flow of carriers. These barriers reach a maximum when all the charge traps at the interfaces are filled, at a critical donor concentration $N_C$. Figure 6 demonstrates what happens to the barrier at various values of the donor concentration for an $n$-type sample.

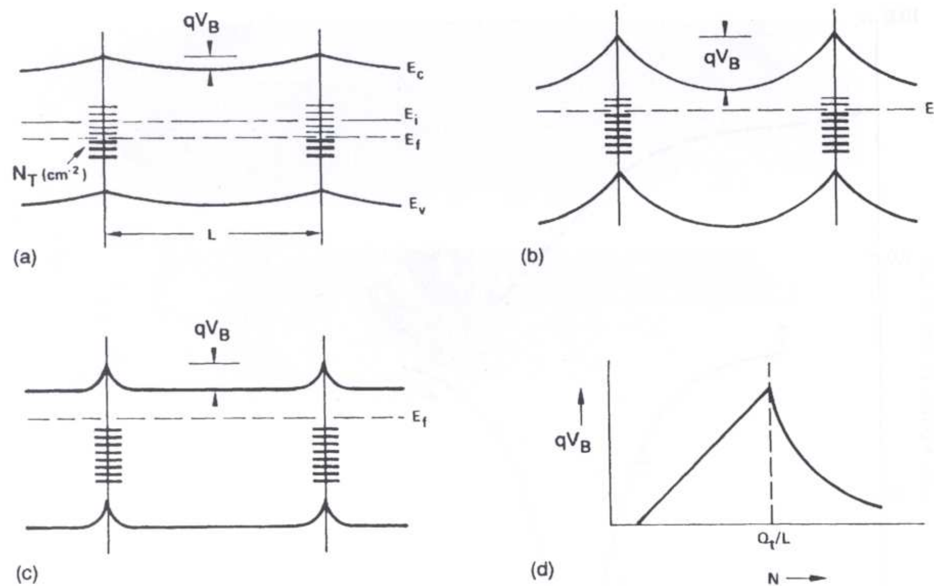


Figure 6: Shown are the energy band diagrams for dopant concentrations a) *below* $N_C$, *at* $N_C$, and *above* $N_C$. From [10].

The simplest way to reduce the effects of these defects is to passivate them. This can be done by introducing hydrogen into the film, which passivates dangling and strained Si bonds at the grain boundary interface. The mechanism is identical to that in a-Si:H. Hydrogen passivation is therefore a key step in producing quality poly-Si films. So while hydrogen is detrimental to the crystallization process (which will be discussed later), it is actually beneficial afterwards. Hydrogenation of the films requires a high-temperature processing PECVD step at 350$^o$C, which is fine for glass substrates but too hot for most plastics.

Increasing the grain size is also an important method of decreasing the effect of grain boundaries, thus increasing the conduction in poly-Si, and this is currently where a lot of research is centred.

# 3 Processing

Poly-Si can be created by a number of different techniques. And within each technique there are many possible variations to the processing parameters. There are two main techniques, direct deposition and indirect deposition. Direct deposition is done using low-pressure chemical vapour deposition (LPCVD). This requires processing at temperatures above $600^o$C, however, making this technique incompatible with low-temperature substrates. These direct-deposition techniques also lead to poly-Si with small grain sizes, columnar structure, and poor electrical characteristics ($\mu \approx 5\ cm^2\ V^{-1}\ s^{-1}$) [8]. Poly-Si has been deposited directly at $555^o$C by Miyasaka [11] and in the $400^o$C range using hot-wire CVD (HWCVD) or PECVD with silane as well as tetrafluorosilane ($SiF_4$) [8].

Indirect deposition can be done using solid-phase crystallization (SPC), metal-induced crystallization, or by laser crystallization of a-Si films. SPC requires tremendously long annealing times (up to two days) at high temperatures ($600^o$C) in Argon gas [5]. Crystallization is done using a precursor a-Si film, which is then melted by various techniques and allowed to cool from the melt, which causes crystals to nucleate in the film. Crystallization by laser beam heating will be the focus of this report. Indirect poly-Si growth by laser crystallization is much more compatible with low-temperature substrates because the film can be heated very quickly, preventing the glass/plastic substrate from melting.

Since laser crystallization is really the only viable processing method for poly-Si on low-temperature substrates, possibly flexible substrates, it will be the chief focus of this paper. Creating a poly-Si via laser crystallization requires two main steps: deposition of precursor a-Si or a-Si:H film, and laser crystallization of the a-Si film. Some other steps may or may not be needed, depending on the exact process used.

## 3.1 Precursor a-Si Film for Laser Crystallization

In order to form poly-Si films on low-temperature substrates, an amorphous silicon layer must first be deposited, which will later be crystallized by the laser beam. The most common techniques are low-pressure chemical vapour deposition (LPCVD), plasma enhanced chemical vapour deposition (PECVD), and sputtering.

LPCVD is done at about $550^o - 700^o$C, which makes it suitable for deposition on some glasses, but incompatible with flexible plastics, due to their low melting points (an ideal plastic is Polyester (PET), which has a maximum processing temperature of $120^o$C).

a-Si can be deposited using PECVD at temperatures as low as $250^o$C, and so it is the favoured processing technique for low-temperature poly-Si. PECVD a-Si:H can be used as a poly-Si precursor for integration of poly-Si with a-Si:H devices on the same substrate;

however, its high concentration of hydrogen (about 10 at.%) can lead to ablation and cracking of the film upon crystallization, due to the rapid out-diffusion of hydrogen. This problem is easily solved because hydrogen diffuses out of the film completely at a temperature of 350$^o$C. Therefore, performing a thermal anneal before crystallization, or using low-intensity laser pulses can dehydrogenate the film. For low-temperature plastic substrates, PECVD has been demonstrated at far lower temperatures than the usual $250^o - 300^o$C range, as low as 120$^o$C [12].

The precursor a-Si films should be as amorphous as possible, in order to minimize the number of nucleation sites during the crystallization stage. It is also advantageous to have low hydrogen content, or no hydrogen at all present in the film, in order to eliminate the dehydrogenation step.

## 3.2 Laser Crystallization

Laser crystallization is most often done using pulsed lasers, although continuous-wave (CW) lasers had been used in the past; however, with CW lasers, the substrates are heated to well above 600$^o$C, which makes this incompatible with low-temperature substrates [9]. (Some work has been done recently with CW lasers and has shown promising results at temperatures below 450$^o$C [7]). Pulsed lasers provide rapid heating and cooling of the a-Si film, without causing the underlying substrate to melt.

### 3.2.1 Excimer Lasers

Rare-gas halogen excimer lasers are used for their short wavelength in the UV band, and their ability to produce short high-intensity pulses. ArF (193 *nm*), KrF (248 *nm*), and XeCl (308 *nm*) are the gas mixtures most commonly used in these lasers for laser crystallization of amorphous silicon. XeCl is the most commonly used excimer laser. The optical skin depth of a-Si at these wavelengths is about 7 *nm*, and the films usually have a thickness of about 100 *nm*. This gives the substrate little chance to heat up, and any heating of the substrate is due entirely to thermal diffusion through the a-Si layer. Using lasers in the UV band is also advantageous because a-Si is highly absorptive in the UV, whereas most glass substrates are not.

### 3.2.2 Solid-state Lasers

More recently, other lasers have been used to produce very high-performance poly-Si thin-film transistors (TFTs). Dassow reports using a Nd:$YVO_4$ laser and achieving TFTs with a

channel mobility of 410 $cm^2\ V^{-1}\ s^{-1}$. This was achieved using a sequential lateral solidification (SLS) process which will be discussed later in Section 5.2.2. For the rest of this paper, it will be assumed that excimer lasers are used, unless otherwise noted.

### 3.2.3 Optical Systems

Some optical processing in needed to ensure that the beam profile is ideal. Usually the beam is passed through a homogenizer which creates a top-hat or mesa profile of the beam. The homogenizer flattens out the profile, however, it also creates many interfering plane waves. This creates an interference pattern with spacing on the order of 10 $\mu m$ which is comparable to device sizes [9]. Focussing lenses are also required to focus the beam to the desired spot size.

## 3.3 Process Parameters

There are many different techniques used to melt the a-Si films and cause crystallization using lasers. There are many parameters which can be varied, including pulse time, beam power, spatial extent, repetition rate, total number of pulses, and scanning rate.

**Pulse length** Pulses usually last between $20-200\ ns$ and this length depends on the laser power of the pulse, and is varied to achieve a certain laser fluence.

**Pulse Intensity** The total energy contained in the pulse is equal to the integral of the pulse's power over time. The energy in the laser's pulse greatly influences the growth progress because it determines the temperature profile in the a-Si film.

**Spatial extent** Spatially, most lasers illuminate an area of about $2 \times 2\ mm^2$ up to $10 \times 10\ mm^2$. Normally the beam intensity is flat, other many other techniques have been tried, in order to fine-tune the thermal gradient in the material.

**Repetition rate** The repetition rate does not affect the quality of the poly-Si as long as the sample cools to room temperature before the subsequent pulse is applied. In practise, rates of $0.5 \rightarrow 50Hz$ are used.

**Total number of pulses** The number of pulses helps the growth of large grains in the material, improves homogeneity, and reduces surface roughening of the film. The number of pulses can vary between $1-100$ or perhaps even more. Usually, however, 100 is enough, and after that, the film does not change much [5].

**Step size** Scanning step size is another factor which influences grain structure. Large step sizes (just less than the diameter of the beam), as well as small step sizes (about 1/20th of the beam diameter) have been attempted. Using a small-step can help produce large, elongated grains, as well as improve the homogeneity of the grains.

# 4 Grain Growth Process

## 4.1 Heat Diffusion Equation

The basic procedure involved in growing grains of crystalline silicon involves heating up the a-Si film above its melting point using short pulses of energy from a laser beam. The film is heated up and cooled so quickly that the substrate below does not have time to heat up past it's melting point. The heating of the substrate can be fully described by the heat diffusion equation [8], which for one-dimension is:

$$\frac{\partial T}{\partial t} = \frac{1}{\varrho C_p}\frac{\partial}{\partial z}\left(k\frac{\partial T}{\partial z}\right) + \frac{\alpha}{\varrho C_p} I(z,t), \tag{1}$$

where $\varrho$ is the density of the film, $C_p$ is the specific heat, $k$ is the thermal conductivity, $\alpha$ is the optical absorption coefficient, and $I(z)$ is the optical poser density and

$$I(z) = I_0(1-R)exp(-\alpha z), \tag{2}$$

where $I_0$ is the incident power density and $R$ is the surface reflection coefficient. As a simple example, from this equation, one can determine the threshold pulse energy required to raise the surface of an a-Si film to its melting point of $1418 \pm 40\ K$. This threshold energy, dubbed the surface melt threshold is given by

$$E_T = \frac{(T_m - T_0)\sqrt{\pi}\varrho C_p \sqrt{D\tau}}{1(1-R)} \tag{3}$$

where $\tau$ is the pulse duration, and $T_m$ is the melting point. This is only one example of a specific laser energy threshold. There is also an energy threshold for when the entire a-Si layer reaches its melting point (melt-through fluence). Many researchers have used computer modelling to try to predict temperature profiles within the sample upon laser heating. The more advanced laser crystallization techniques attempt to model the temperature distribution in the sample, by tweaking the power distribution of the laser in space and time. By fine-tuning the laser power distribution, and hence the temperature distribution in the sample, it is possible to achieve the most optimal grain size and also can help to better pinpoint the location of the grains in the silicon.

## 4.2 Grain Growth Dependence on Laser Fluence

There is no factor which affects the grain growth in poly-Si more than the laser fluence. It is possible to get even larger grains by using other, more newer and exotic techniques, however, without having the proper fluence to begin with, creating large grains would not be possible at all. With the proper fluence, the sample can be heated above the melting point throughout the thickness of the film, and grain growth may proceed from a small number of nucleation sites to form large grains.

Laser fluence is normally measured in $mJ/cm^2$. So, it is the integral of the laser's power with respect to time, or the total energy in the pulse which is important. Specific laser fluences for some given film and laser properties divide up the growth process into four major regimes. These four regimes are shown in Figure 7. This graph was produced by the

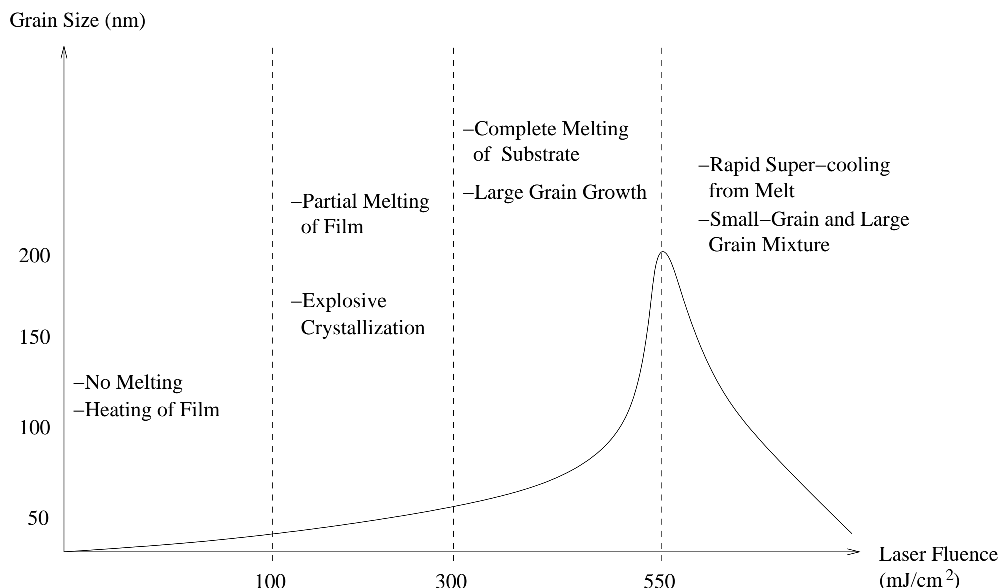


Figure 7: Qualitative plot of grain growth versus laser fluence for a Gaussian beam of 20 $ns$ at full-width half-maximum (FWHM) on 100 $nm$ of Si on a quartz substrate.

author of this report, however, the values for laser fluence are provided by Boyce and Mei [9, 13] for the case of a 20 $ns$ laser pulse on 100 $nm$ of Si on top of a quartz substrate. At laser fluences below $\approx$ 100 $mJ/cm^2$, the surface of the a-Si film is not even melted, and some heating of the a-Si film is all that occurs. Using equation 3, one can find the surface melt threshold fluence to be about 100 $mJ/cm^2$ for this particular laser and film. The first regime is really not a regime of crystallization at all, and so it does not deserve a category on its own.

The reason grain growth is so important is that it determines the mobility of the material, since the grain boundaries are the main limiting factors which limit the conduction in poly-

Si, as discussed in Section 2 above. From Figure 8, it can be seen that the mobility is very proportional to the grain size.

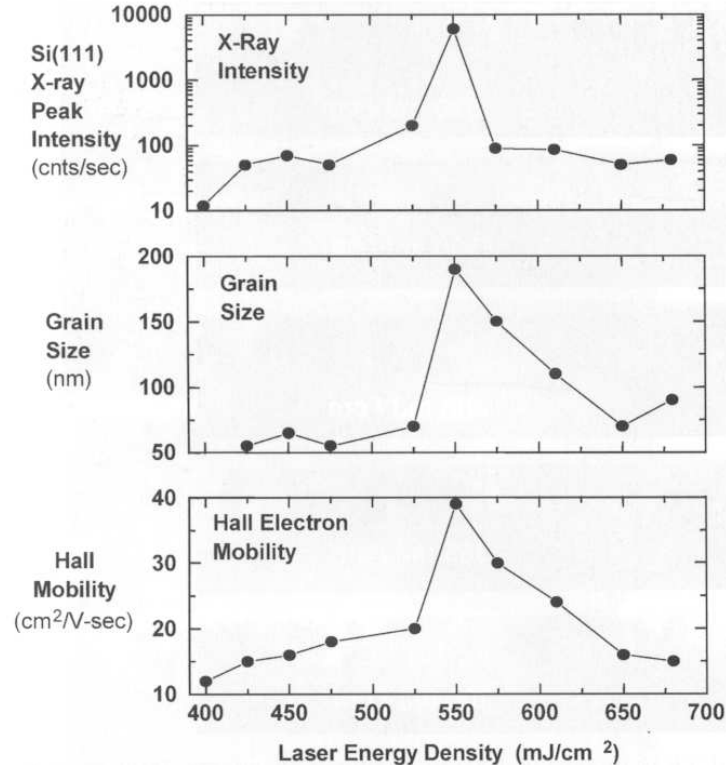


Figure 8: The laser fluence dependence of the Si(111) X-ray peak intensity, the average grain size, and the electron mobility [9].

### 4.2.1 Partial-Melting Regime

At fluences above 100 $mJ/cm^2$, the film is partially melted, although not completely. Some crystallization occurs near the surface, although the grain size is quite small. This is illustrated in Figure 9. At these fluences, there is just enough energy to melt the surface of the film and turn a-Si into molten Si. a-Si has a melting point of around $\sim 1400\ K$. The melting temperature of crystalline silicon is slightly higher, at 1687 $K$. The melted silicon at the surface nucleates due to the large source of nucleation sites at the continuous unmelted a-Si interface. The molten film therefore crystallizes into supercooled poly-Si. Crystalline silicon has a latent heat of 1800 $J/g$, and this heat gets released when this supercooled layer solidifies. This latent heat is sufficient to melt the underlying a-Si, because a-Si has a latent heat of only $\approx 1300\ J/g$. This newly melted a-Si layer is also supercooled, and the process repeats, as a fine layer of molten silicon propagates downward through the film. This process is called "explosive crystallization" [9]. Explosive crystallization is characterized by a

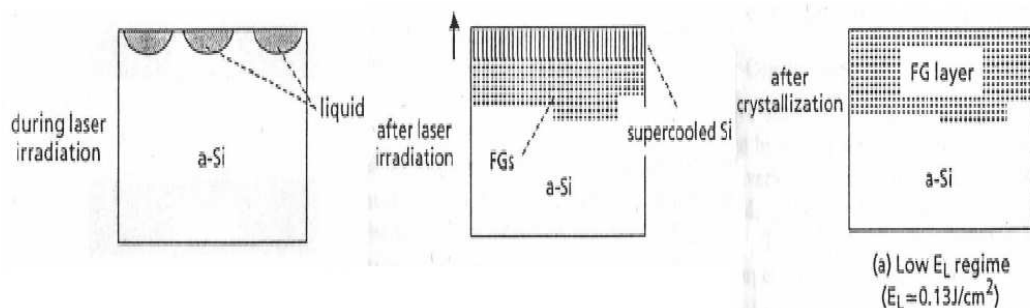


Figure 9: Picture of grain growth in a-Si sample with low-level laser heating ($100 < F \ll 300$ $mJ/cm^2$ for example in question). From [14].

fast-moving molten layer. Since this rapid cooling and and solidification proceeds so quickly, the poly-Si grain size is very fine-grained.

As the laser energy is increased further, the region of molten silicon near the surface is larger, and this allows larger grains to grow upward from the seeds at the interface into large columnar grains, as shown in Figure 10. The upper region forms larger crystals because this region is cooled much more slowly. The layer below the substrate experiences explosive crystallization as described above, which means the poly-Si formed below above the substrate interface will be fine-grained poly-Si. Boyce and Mei have some cross-section TEM photos

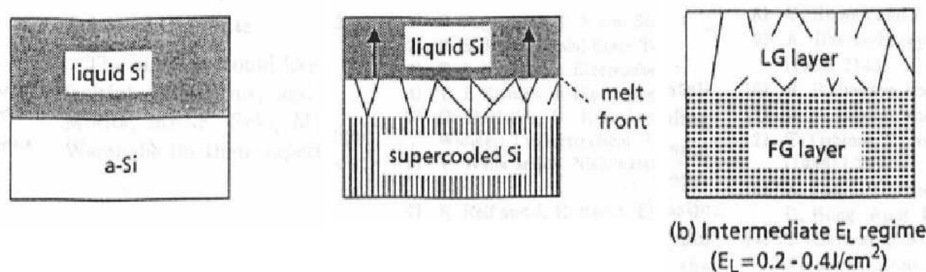


Figure 10: Picture of grain growth in a-Si sample with low-level laser annealing, above melt-through threshold ($F < 300$ $mJ/cm^2$ for example in question). From [14].

of 100 $nm$ laser-crystallized silicon on quartz in this growth regime. These photographs are shown in Figure 11. The pictures in Figure 11 clearly show the make-up of the material under low laser fluence, as described above. In Figure 11 a), there is no crystallization of the film. In Figure 11 b), there is some explosive crystallization near the surface, some unmelted a-Si near the substrate interface, and no large grains. In Figure 11 c) there is some large grain-growth near the surface, as well as explosive crystallization which extends all the way to the substrate interface below. And finally in Figure 11 d), there is large columnar grain growth in the upper half of the material, and explosive grain growth in the bottom half. Full

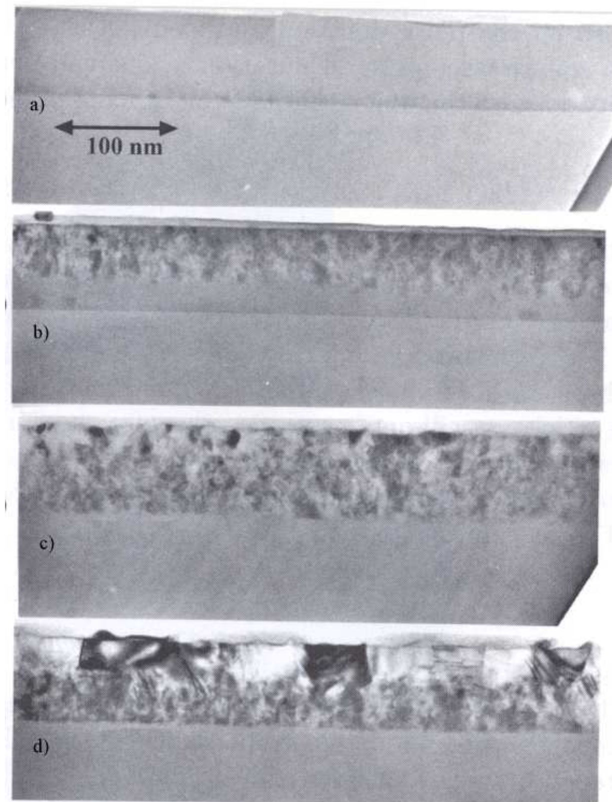


Figure 11: Pictures of a laser annealed sample at four different fluences: a) Just below the surface melt threshold of 100 $mJ/cm^2$, b) 100 $mJ/cm^2$, c) 200 $mJ/cm^2$, and d) 250 $mJ/cm^2$, just below the melt-through fluence of 300 $mJ/cm^2$. From [9].

melt-through still has not been achieved, although due to the explosive crystallization effect, the entire film did in fact "melt".

### 4.2.2 Complete Melting Regime / Sub-Critical Regime

At a certain critical fluence, the entire film will be melted. For the example being discussed, this threshold fluence is $\approx 300\ mJ/cm^2$. However, this threshold value was obtained qualitatively, by looking at cross-section TEM views of the film. Figure 12 below documents the growth of polycrystalline silicon grains above the melt-through fluence. According to Im

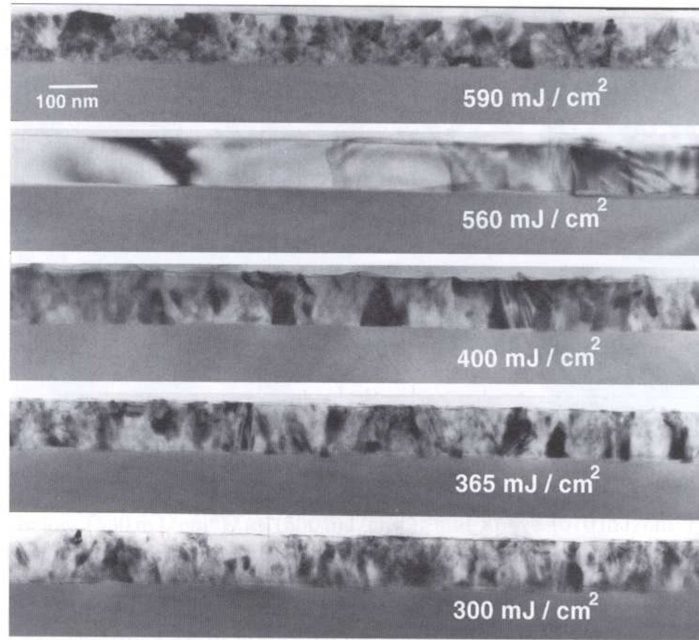


Figure 12: Cross section TEM images from [9, 9] for laser fluences above the melt-through fluence of $\approx 300\ mJ/cm^2$.

[15], although the film may appear to be fully melted, there are still many unmelted islands of solid amorphous silicon at the interface with the substrate. These unmelted "islands" are nucleation sites for poly-silicon grain growth in the film.

### 4.2.3 Critical Regime

As the laser fluence is increased even further, the number of discrete unmelted islands of solid silicon at the interface will be diminished as they are destroyed due to the increased laser energy. This reduction in the number of nucleation sites will mean that fewer grains will nucleate from the interface, and hence the grains will be larger. For the example being discussed, this critical fluence is $\approx 550 - 560\ mJ/cm^2$. This dramatic increase in grain size

near the critical fluence is seen in Figure 12, where the grains are very large at the fluence of 560 $mJ/cm^2$.

#### 4.2.4 Super-Critical Regime

At high laser fluences, above the critical fluence value, the grain size actually decreases. In this regime, there are no longer any discrete islands of solid silicon at the interface, and the entire a-Si film is melted. When this film cools, it forms homogeneous small-grained material. The reason for this behaviour is a large increase in the number of nucleation sites in the material. There are a couple of different ways that this can occur. One method is by the homogeneous nucleation from a supercooled melt, before grain growth from the substrate interface can occur [15]. Since the main source of nucleation sites at the interface (unmelted a-Si) is no longer present, this is a plausible explanation. Another source of homogeneous nucleation is the creation of a large number of nucleation sites at the interface due to substrate damage. At very high fluences, a high degree of roughening has been observed at the interface. This roughening, or damage to the substrate interface, can provide a large number of nucleations sites for homogeneous nucleation to occur. Figure 12 also shows the super-critical fluence regime in the uppermost photograph at a fluence of 590 $mJ/cm^2$. It is undesirable to have material subjected to fluences in this regime. The best quality poly-silicon material is obtained at fluences around the peak critical fluence or below this value.

### 4.3 Surface Roughening

Surface roughening is a problem in poly-Si films created by laser crystallization. Figure 13 shows a 100 $nm$ thick film which has been irradiated at the critical fluence. The size of the hillocks in this micrograph are in some instances almost as large as the film is thick. Many causes have been cited in the literature for surface roughness, such as, the difference in latent heats between amorphous and polycrystalline silicon, hydrogen evolution in laser crystallized a-Si:H, and positive feedback of optical interference effects. The most recent explanation has been the propagation of capillary waves excited by the volume change at the melt transition interface [16].

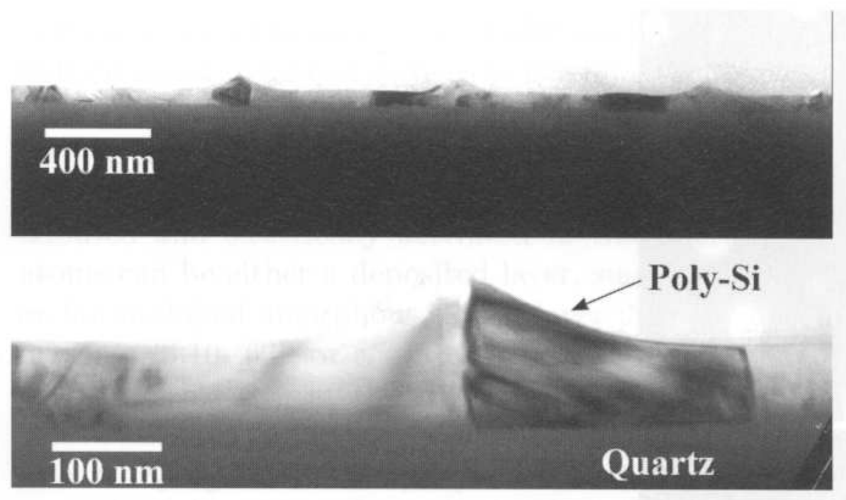


Figure 13: TEM micrographs showing large hillocks formed at grain boundary, which lead to surface roughening. From [9, 9].

# 5 Increasing Grain Size and Improving Homogeneity

One of the main problems with polycrystalline silicon fabrication by laser annealing is that devices created on the poly-Si film have many inconsistencies in their device parameters due to the inhomogeneity of the film. These non-uniformities arise directly from the fact that the grain growth is very sensitive to the laser fluence. Although the excimer laser beam is normally passed through a homogenizer to create a top-hat laser energy profile in space, the homogenizer creates many interfering plane waves, which means that the energy profile can never be completely flat. Some parts of the beam will therefore be closer to the critical laser fluence than others. This leads to some regions having large grains and others having small grains. Poly-Si devices created on these films have large variations in their device parameters. In order to reduce the variability among devices, it is necessary to perform laser annealing at temperatures below the critical fluence. This is a trade-off between uniformity and performace. Figure 14 shows some experimental data, which shows increasing device mobility near the critical fluence, and the large error bars illustrate the poor uniformity in this region. The error bar at the peak actually overlaps the error bar at the next lowest energy fluence level.

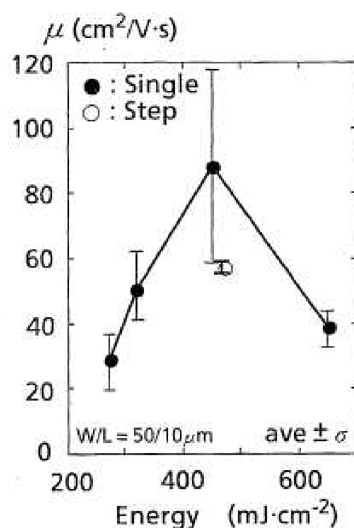


Figure 14: Device mobility versus laser energy fluence for a single-step anneal, and a “step” anneal. From [17].

## 5.1 Basic Techniques

Figure 14 as well as Figure 15 also shows one of the most basic techniques to improve uniformity, which is to anneal the material at multiple energy fluences. In Figure 15, the

material was annealed at two different fluences, and it is shown here that uniformities caused by the beam profile itself are reduced, if the material is illuminated with two pulses of increasing fluence. Of course, as well as decreasing the variation in the grain size, the average grain size is decreased as well, as seen in Figure 15.

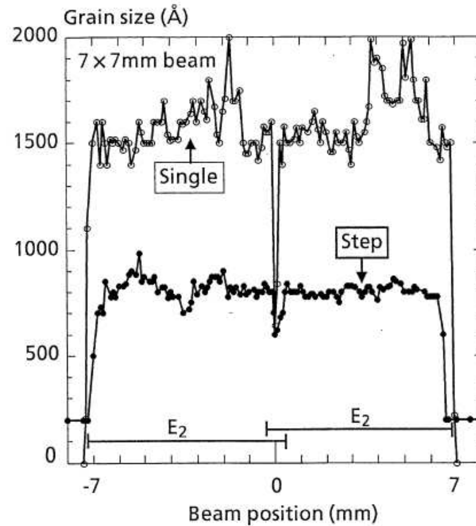


Figure 15: Grain size versus beam position for a single-step anneal, and a "step" anneal. From [17]

Another commonly used technique is small-pitch scanning. This is when the beam is scanned across the sample at a pitch smaller than the beam size, and one of more pulses are applied to the film at each step. Figure 16 shows how the uniformity of grain size is improved with small-pitch annealed film, and also that the average grain size is decreased. In this type of annealing, an area the size of the beam spot is melted, then the sample is translated by a fixed distance of equal to the pitch size. When the sample is annealed the second time, only the newly irradiated region is melted, because the original region which solidified into poly-Si has a higher melting point than the a-Si. Most of the melting is therefore done by only one edge of the beam, which will not be as inhomogeneous as the entire beam. There is also an averaging effect, because each section of the sample will be irradiated multiple times, from varying points on the beam, thus negating any variations in the beam's power.

These techniques can improve the homogeneity greatly, however, poly-Si produced using only these techniques take a big hit in terms of their grain size, and hence mobility (note Figure 14 above, which shows that devices produced at fluences below the peak fluence have mobilities of less than 100 $cm^2\ V^{-1}\ s^{-1}$). More advanced techniques are needed in order to maximize the grain size while keeping the uniformity at an acceptable level.

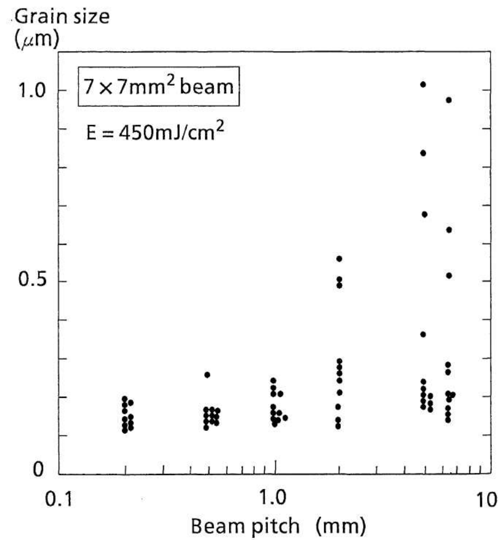


Figure 16: Grain size versus beam pitch. From [17].

## 5.2 Advanced Techniques

There are too many techniques to list here in this report. Only some of the most interesting and most successful techniques will be presented, and so this list is by no means exhaustive.

Most of these techniques have one thing in common. They attempt to control the temperature profile in the sample as it cools. This can be done by controlling the location of heat sinks, or controlling the laser intensity profile itself.

### 5.2.1 $Si0_2$ Membrane Method

Choi has pioneered a method, whereby the underlying substrate is thinner in the irradiated area of the a-Si film, and is thus called a "membrane" (see Figure 17). The sample is illuminated above the membrane region, causing the a-Si to melt. Vertical conduction through the thin substrate occurs quickly, and since the $SiO_2$ layer is very thin just below the irradiated area, thermal conduction in the lateral direction then dominates. Due to this lack of vertical conduction, the melted silicon cools primarily from the lateral direction, and since this "membrane" is made to be quite long, the melted silicon can remain melted for a long period of time. Nucleation of grains begins at the edge of the membrane and propagates inward, forming long lateral grains, which meet in the centre of the membrane. Choi obtained grains of up to 70 $nm$ in length and a few $\mu m$ in width, and TFTs constructed with channels parallel to the grains achieved electron mobilities of 600 $cm^2\ V^{-1}\ s^{-1}$ [18].

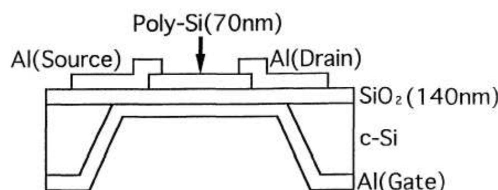


Figure 17: Physical setup for poly-Si created using $SiO_2$ membrane. From [18].

#### 5.2.2 Solid-State Lasers

Dassow et al. have done some research on laser annealing using a pulsed solid-state Nd:$YVO_4$ laser, and have produced some decent results. They use an elongated laser beam profile, and translate their sample at steps of 1/24th the laser spot size, as show in Figure 18. After

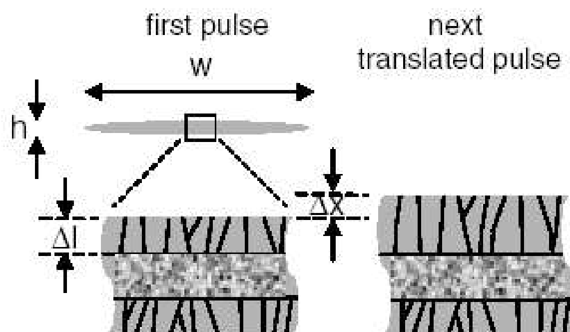


Figure 18: Illustration of stepped annealing procedure. From [3].

the sample is translated after every pulse, grains are nucleated in the newly melted region from the previously solidifed poly-Si. Large grains can thus grow in the lateral direction. Other advantages of their technique are an apparently higher throughput processing, no need for vacuum conditions as in excimer laser annealing, and a resilience to power fluctuations of up to 30% [3]. With this technique, Dassow created TFTs with electron mobilities of 410 $cm^2\ V^{-1}\ s^{-1}$ [3].

Hara has done some research on solid-state laser annealing as well, only he used a continuous wave (CW) Nd:$YVO_4$ laser, as opposed to a pulsed laser. Advantages of this technique include, wide range of scanning speeds and output laser power (see Figure 19), making it easier to form large grains, stable continuous laser power, and directional solidification caused by laser scanning [7]. Hara cites a 1% variability in the output power of the CW solid-state laser, which is much better than an excimer laser [7]. Hara obtained TFTs with an electron mobility of 556 $cm^2\ V^{-1}\ s^{-1}$.

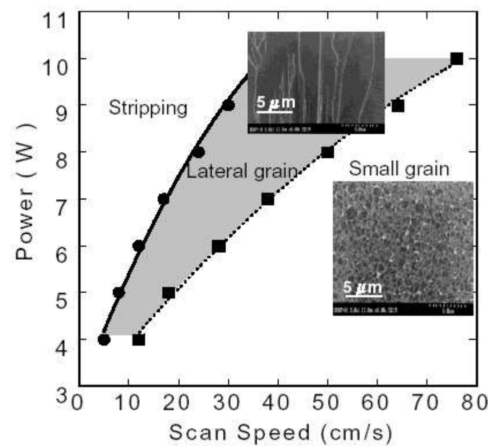


Figure 19: Relationship between structure of grains and different levels of laser output power and different scanning speeds. From [7].

### 5.2.3 Masking

Using masks to control which regions of the amorphous silicon are irradiated is one of the most successful methods to control the location of grains. Mariucci has developed an innovative technique, which provides excellent grain location control. A mask is used to control which regions are illuminated with laser light, as shown in Figure 20. This technique is ac-

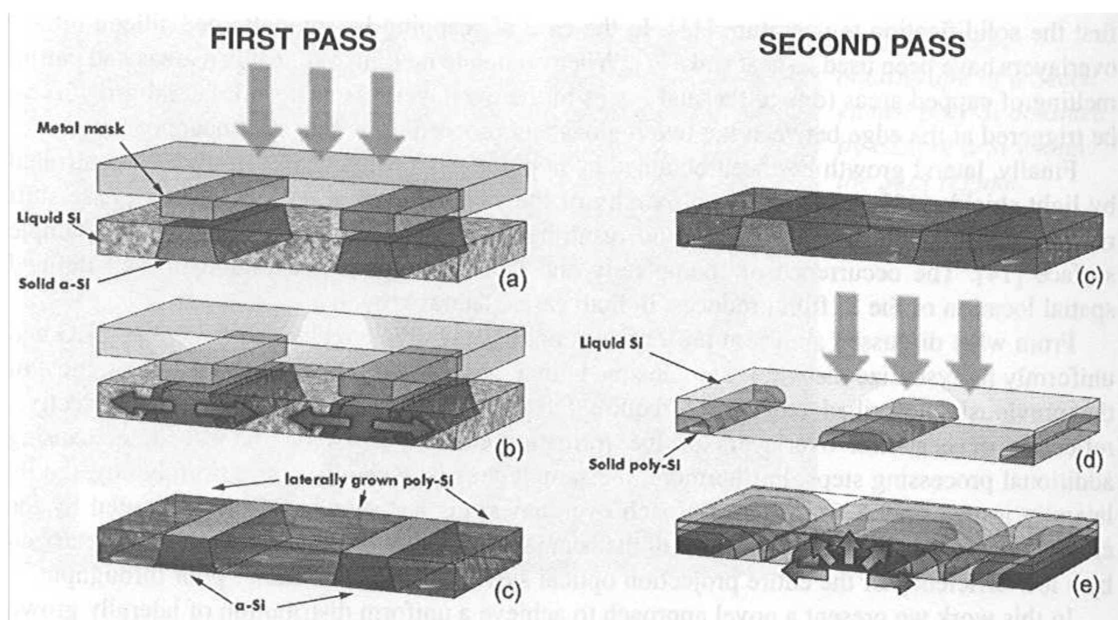


Figure 20: Graphical illustration of two-pass masking technique. From [19]

tually quite simple. After the first laser pulse (with the mask in place), grains nucleate from the unmelted regions and propagate in toward the melted region, and adjacent grains will

meet along a single grain boundary. On the second pass (with the mask removed), the entire sample is illuminated, but melting only the amorphous silicon, which has a lower melting point, and partially melting the poly-Si formed in the first pass. Grains now nucleate from the grains which were created during the first pass, and again, adjacent grains meet along a single grain boundary. All the grain boundaries are somewhat pre-determined, and the grain size is a decent size, because lateral solidification was controlled due to the "cool zones" or unmelted silicon which act as heat sinks. Figure 21 shows the end material produced using the two-pass technique. The material shows excellent spatial control of the grains and large grains as well.

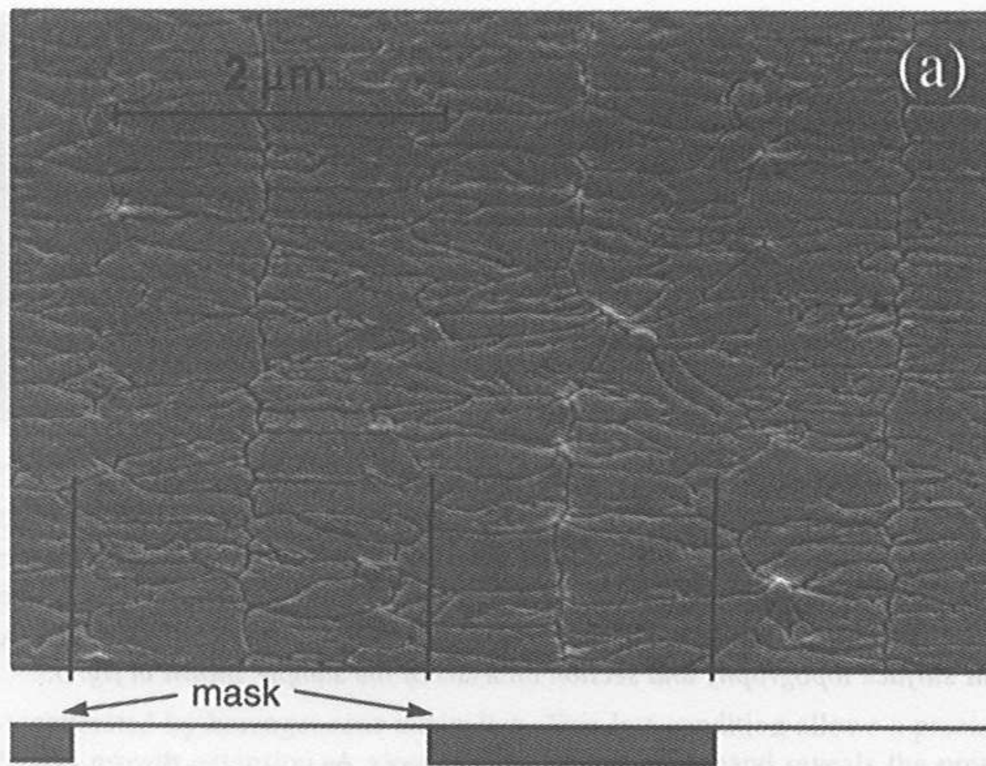


Figure 21: Micrograph of poly-Si material created using the two-pass masking technique. From [19].

Initially, it was found that surface roughness was a problem with this technique. However, using multiple pulses after the mask is removed, instead of just one pulse, has been shown to reduce the surface roughness significantly [19].

# 6 Poly-Si Devices

In order to make poly-Si devices, one needs to look at the big picture, before deciding which process is best. For example, if poly-Si devices are to be created on the same substrate as a-Si:H devices, then a process must be used which works well with both materials.

## 6.1 Poly-Si TFTs

Poly-silicon TFTs, created by laser annealing, can be manufactured using several different approaches, similar to a-Si:H and crystalling silicon devices. Figure 22 shows three possible processes. In polycrystalline silicon, normally the top section of the material is of better

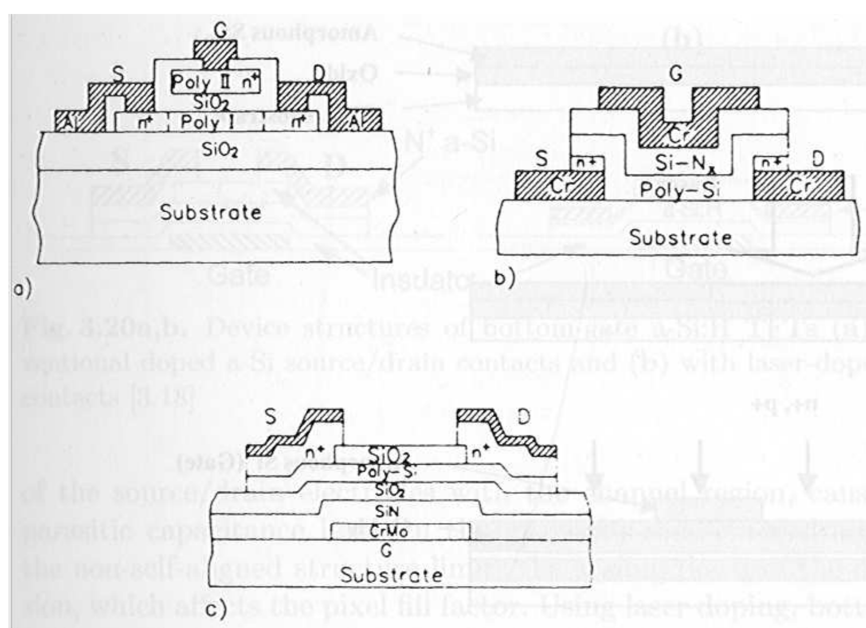


Figure 22: Various processing techniques for poly-Si devices include, a) top-gate coplanar, b) top-gate staggered, c) bottom-gate staggered. From [8].

quality, because this area receives the most energy from the laser and is hence completely melted. The lower section of the material can be prone to having small-grained material due to incomplete melting. The top-gate structure is therefore preferred for poly-silicon TFTs, because most of the current passes through the top section of the poly-Si film, where the mobility is higher. However, the surface of the material can have a very high roughness (in some cases on the order of the thickness of the film), which causes a lot of interface states along the oxide interface.

A bottom-gate TFT avoids the surface roughness problem, however, a new problem is introduced, and that is damage to the oxide and gate beneath the poly-Si film during laser

heating. As a result, lower laser fluences need to be used, which leads to lower mobility material. Most of the conduction takes place in the bottom section of the material, which has lower mobility already. For these reasons, the top-gate structure is preferred for poly-Si devices.

## 6.2 Integration with a-Si:H TFTs

Although pixel switches for matrix arrays could be made with poly-Si, poly-Si leakage currents are too high for this application, and a-Si:H TFTs must be used instead. In a-Si:H TFTs, the bottom-gate has a far better mobility of $\approx 1\ cm^2\ V^{-1}\ s^{-1}$, compared to the top-gate, which has a mobility of $\approx 0.2\ cm^2\ V^{-1}\ s^{-1}$. However, for poly-Si TFTs, the top-gate configuration is better, and the bottom-gate is worse. So which process should be used for integrated a-Si:H and poly-Si processing? Research as shown that in general, the bottom-gate configuration is better for integration of poly-Si and a-Si:H TFTs on the same substrate; however, this may not be the case for all applications.

Figure 23 shows a typical integrated display process. The display is initially pattered with

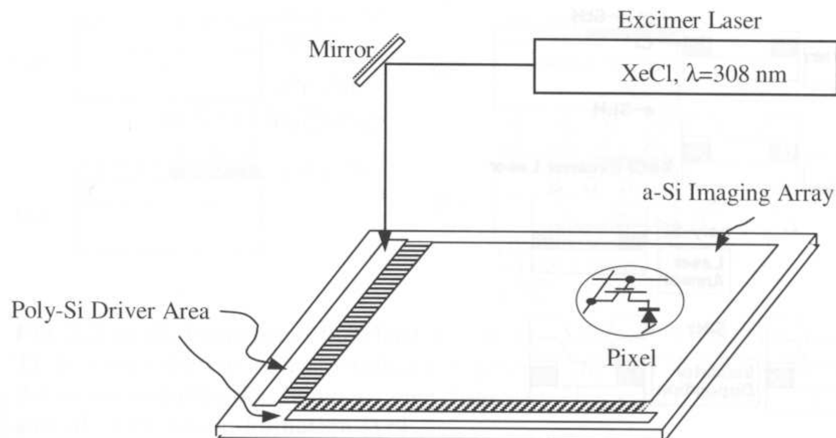


Figure 23: Laser crystallization system for integration of a-Si:H array and poly-Si circuitry on same substrate. From [9].

an a-Si:H active pixel array, and then the external driver areas of the substrate are annealed using a laser, to form poly-Si channels. Being able to anneal the poly-Si circuit in one pass in a single spatial dimension would increase homogeneity a lot. So having the poly-Si circuitry in a linear fashion as shown in Figure 23 is advantageous. This raises another question, what to do about the hydrogen in the a-Si:H during laser annealing? As described in Section 3.1, hydrogen can damage the film if it is present during the laser annealing process. There are many possible solutions to this problem. a-Si with no hydrogen can be the starting material and the poly-Si and a-Si TFTs can by hydrogenated using PECVD after all the processing

is completed. This requires raising the substrate temperature however, to allow hydrogen to diffuse into the a-Si and poly-Si film, which may not work for some low-temperature plastics, although it would for most glasses. Another option is to deposit a thin a-Si layer, and then during the laser annealing process, pulse the laser at low fluences in order to remove hydrogen from the desired areas. Once the hydrogen has left this area of the film, laser annealing can take place.

# 7 Conclusion

Polycrystalline silicon is a material which is sure to have an increasing presence in the electronics of the future. Roll-to-roll electronics on flexible substrates, LCD displays, large-area imaging arrays, and countless other applications will rely on poly-Si for its higher speed of operation and ease of integration with a-Si:H devices. Laser crystallization will be a necessary processing step in order to create poly-Si on the low-temperature substrates of the future. There are still many issues which need to be resolved before large circuits can begin to be manufactured on the substrate instead of in external chips. Laser crystallization needs to be able to create material with sufficient mobility, and with uniformity and repeatability. This is something that has currently only been possible for very small displays such as cell-phone displays and overhead projectors. Ultimately, poly-Si will help make large area electronics more economical, by providing more circuitry on the inexpensive plastic substrate, meaning less need for external crystalline silicon circuits and costly packaging.

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