Bottom Gate TFTs With Channel Layer Deposited by Pulsed PECVD

M.A.Sc. Seminar

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Outline

1. Introduction
   - Motivation
   - Background

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2. Material Characterization
   - Structural Characterization
   - Electrical Characterization

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a-Si:H

Advantages

- Low conductivity
- Deposition over large areas
- Deposition at low-temperature

Disadvantages

- Low electron mobility ($\leq$1 cm^2 V^{-1} s^{-1})
- Hole mobility is prohibitively low, so *p* type devices are not possible
- Poor stability under gate bias stress

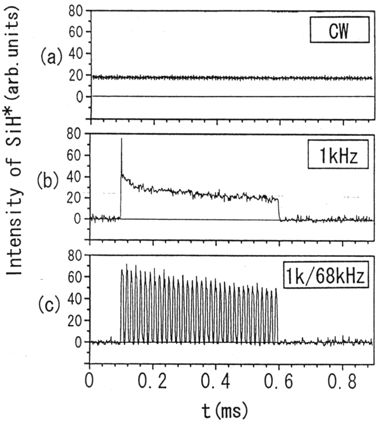
Motivation for nc-Si:H

- Can be deposited using standard PECVD
- Has a crystalline structure which can lead to:
  - Higher mobility ⇒ reduce TFT W
  - Higher stability ⇒ peripheral circuits possible using nc-Si:H [French, 2001]
- nc-Si:H TFTs are definitely a promising improvement over a-Si:H TFTs for LCD applications without the disadvantages of poly-Si TFTs.

Methods of Growing nc-Si:H

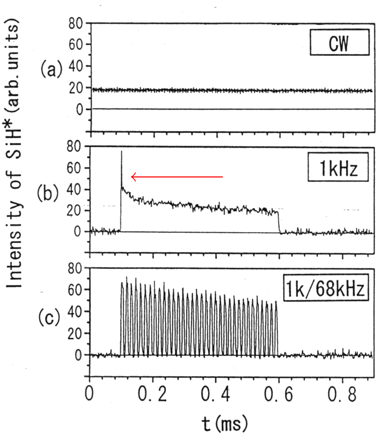
- Thermal and/or laser crystallization
- SiF_4 or $SiCl_2H_2$ PECVD with or without SiH_4 $\Rightarrow$ new gases needed
- Very High Frequency (VHF) PECVD $\Rightarrow$ not scalable due to nonhomogeneous plasma
- Standard SiH_4 PECVD with high H_2 dilution
- Pulsed PECVD with high H_2 dilution
  - Increased growth rate
  - Reduced powder particles
  - Increased degrees of processing freedom

Pulsed PECVD



Two main effects of pulsed PECVD:

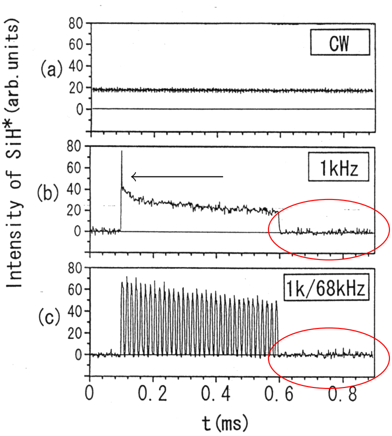
Pulsed PECVD



Two main effects of pulsed PECVD:

- High energy electrons during transient phase leads to increased radical density (increased growth rate of nc-Si:H compared to standard PECVD)

Pulsed PECVD



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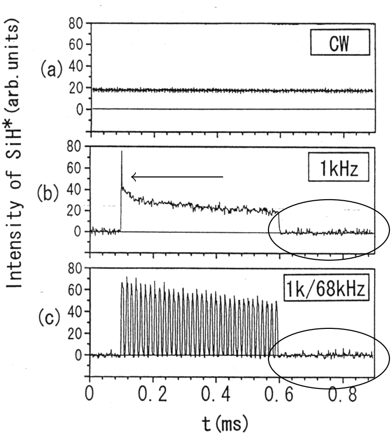
- Turning off plasma allows radicals to escape from chamber, thus reducing powder particle formation

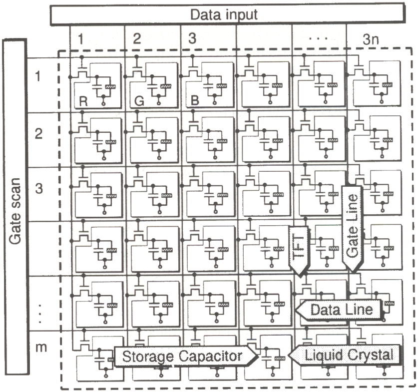
Pulsed PECVD



Two main effects of pulsed PECVD:

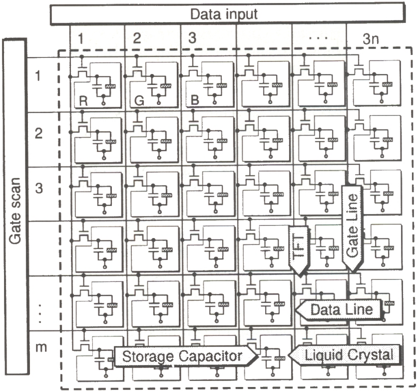
- High energy electrons during transient phase leads to increased radical density (increased growth rate of nc-Si:H compared to standard PECVD)
- Turning off plasma allows radicals to escape from chamber, thus reducing powder particle formation
- Pulsed PECVD provides increased processing degrees of freedom, and is a promising technique for depositing thin film devices such as nc-Si:H solar cells and TFTs

AMLCD Modelling



What effect does an increased mobility have on an LCD display?

AMLCD Modelling



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- Many variables are affected: resolution, refresh rate, display size, fill factor

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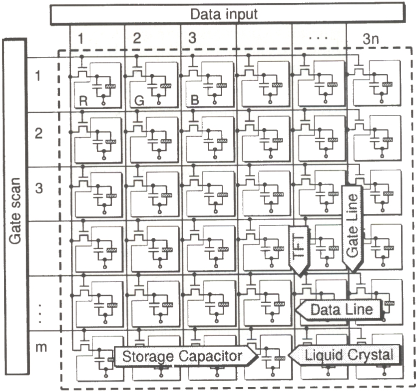

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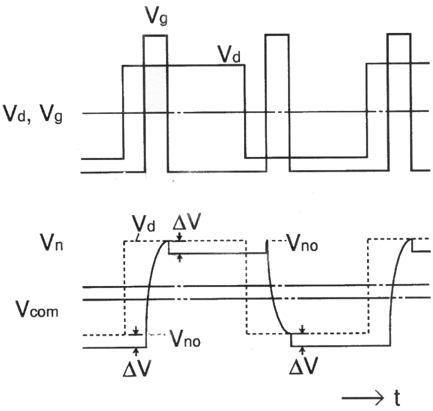

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- Many variables are affected: resolution, refresh rate, display size, fill factor
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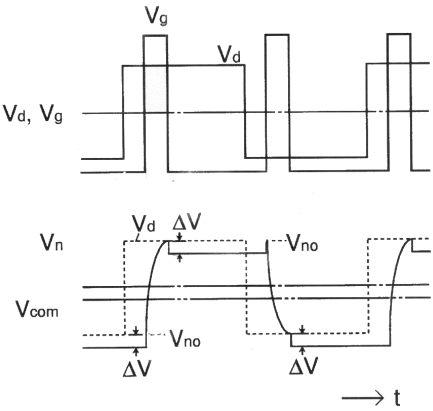
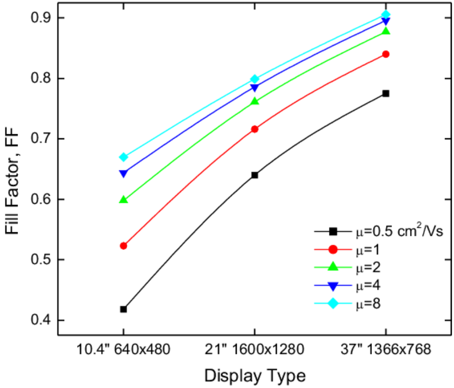


What effect does an increased mobility have on an LCD display?

- Many variables are affected: resolution, refresh rate, display size, fill factor
- Mobility also a function of: TFT size, minimum feature size, capacitance,
- voltages, pixel charging ratio, gate line delay
- Some of these can be fixed or variable

Modelling Fill Factor Increase with Mobility



- Modelling software was written in Python
- 3 displays (10.4″, 21″, and 37″) were simulated to observe the effect of an increased mobility on fill factor
- Fill factor improves (obviously) but relationship depends on display
- There is a limit to how much, due to gate/data lines, and source/drain

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Processing Conditions

Film	Si_4 Flow Rate	H_2 Flow Rate	Power	Pressure
1	20 sccm	0 sccm	2 W	0.4 Torr

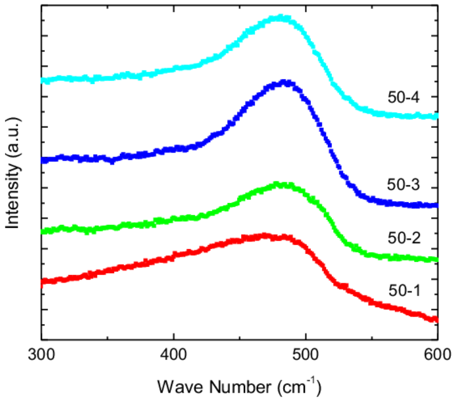
- Film 1 has no hydrogen dilution (a-Si:H)

Processing Conditions

Film	Si_4 Flow Rate	H_2 Flow Rate	Power	Pressure
1	20 sccm	0 sccm	2 W	0.4 Torr
2	4 sccm	100 sccm	100 W	1.8 Torr
3	2 sccm	100 sccm	40 W	1.8 Torr
4	3.5 sccm	100 sccm	100 W	1.8 Torr

- Film 1 has no hydrogen dilution (a-Si:H)
- Films 2-4 have varying degrees of hydrogen dilution (nc-Si:H)

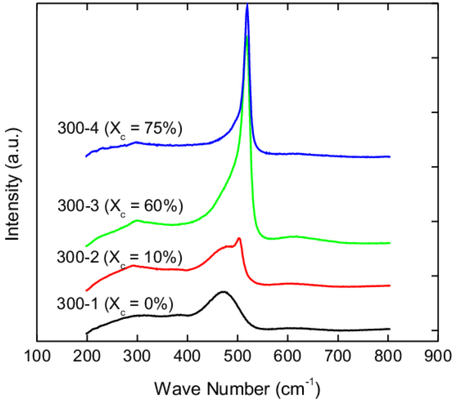
Raman Results for 50 nm Films



- Crystallinity is absent/undetectable
- FWHM is less in 50-3 and 50-4 due to higher bonding order, perhaps due to hydrogen dilution in gas

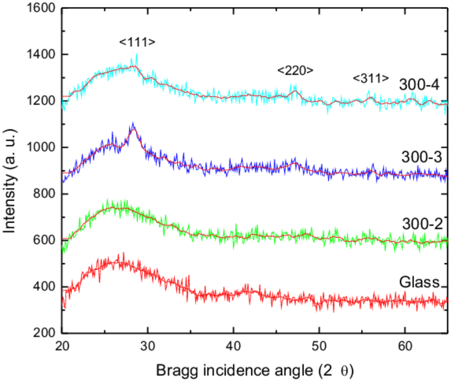
Sample	FWHM (cm^{-1})
50-1	296
50-2	213
50-3	129
50-4	161

Raman Results for 300 nm Films



- 300-1 is a-Si:H (no hydrogen dilution)
- 300-2 slightly crystalline?
- 300-3 has ≈ 60% crystallinity
- 300-4 has ≈ 79% crystallinity

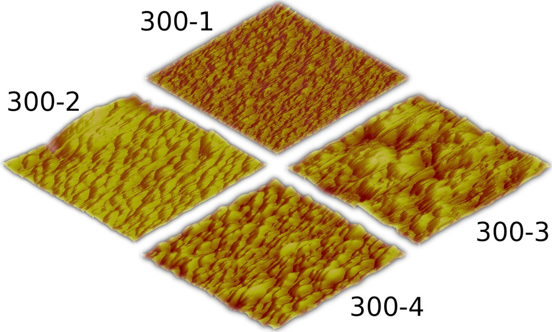
GXRD Results for 300 nm Films



- ⟨111⟩ and ⟨220⟩ predominant

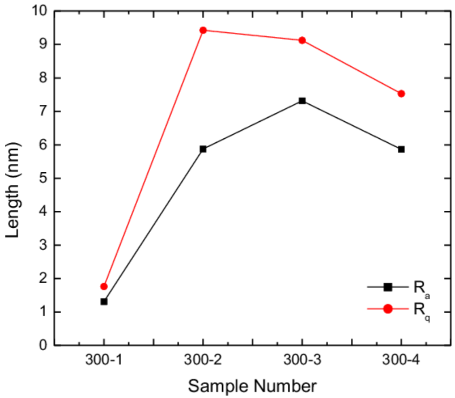
Sample	Plane	d_{GXRD} (nm)
300-3	⟨111⟩	5.0
	⟨220⟩	4.2
300-4	⟨111⟩	7.5
	⟨220⟩	7.1

AFM Results for 300 nm films



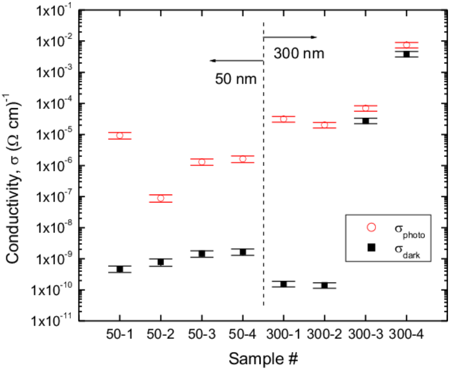
- 1 μm-wide view: 300-3 are 300-4 have higher roughness
- Higher roughness does not necessarily mean higher crystallinity or grain size

AFM - Roughness Extraction



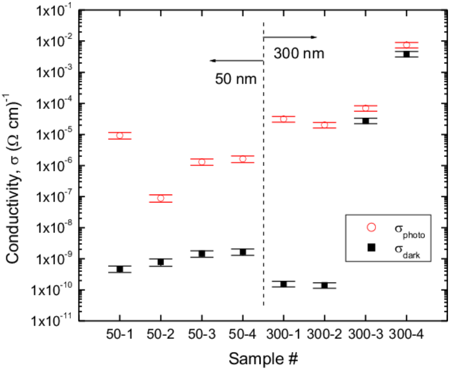
- Roughness is in the range of 6–7 nm for samples 300-2, 3, and 4
- Similar to grain size of 4.2–7.1 nm obtained from GXRD

Conductivity in 50 nm samples



- 2-probe conductivity (1.3 mm × 10 mm gap)
- 50 nm films have σ_{dark} on the order of $10^{-9}\,(\Omega \cdot cm)^{-1}$, similar to that of the a-Si film, 50-1.
- Lower photo conductivity in 50-3 and 50-4 may be due to more ordered structure

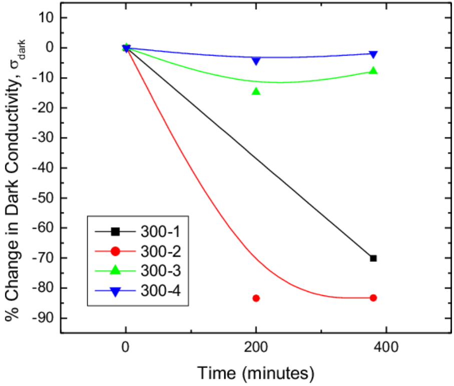
Conductivity in 300 nm samples



- 300-1 and 300-2 has low σ_{dark} and high σ_{photo}, typical of a-Si films
- 300-3 and 300-4 show a higher σ_{dark} and very small $\sigma_{photo}/\sigma_{dark}$ which is expected for high crystallinity films
- *n*-type behaviour may be due to oxygen contamination along grain boundaries

Stability Against Light-Soaking

Dark conductivity



- Amorphous films 300-1 and 300-2 show 70%–80% degradation in conductivity
- Crystalline films 300-3 and 300-4 show little change in conductivity

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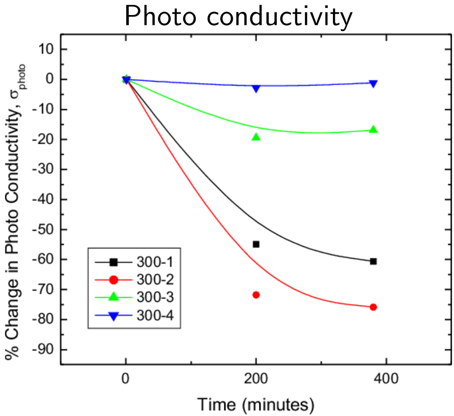
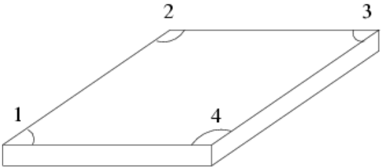


- Amorphous films 300-1 and 300-2 show 70%–80% degradation in conductivity
- Crystalline films 300-3 and 300-4 show little change in conductivity
- Same behaviour for photo conductivity

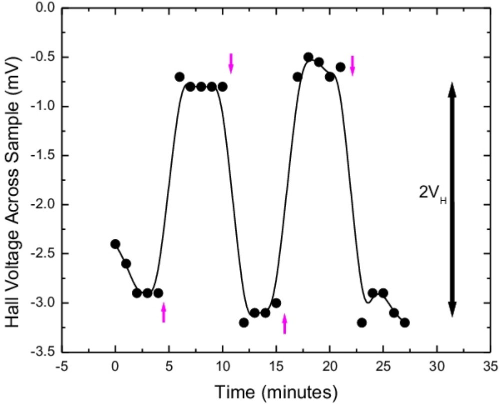
Hall Measurement Setup at University of Toronto

Hall Sample



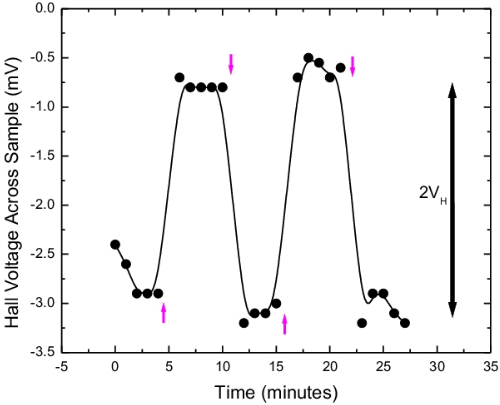
- Magnet capable of $\approx 0.43\,\mathrm{T}$
- Hall sample was 1 cm × 1 cm with four 1 mm contacts deposited on corners
- Sample mount was temperature controlled to 25 °C which was helpful in controlling drift
- 100 V was applied to contacts 1 and 3
- The Hall voltage was measured by reversing magnetic field and measuring the change in V_{24} which is equal to $2V_H$

Hall Mobility Measurements



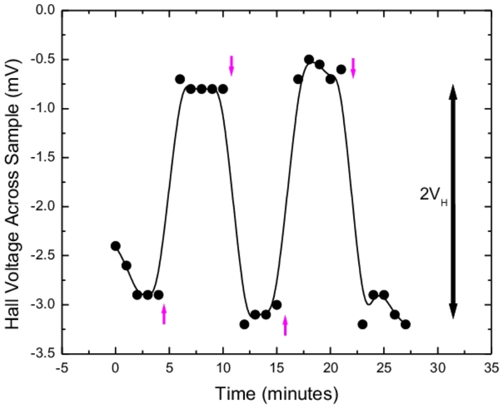
- $R_S = \rho/t$
- $V_H = 1.15\,\mathrm{mV}$

Hall Mobility Measurements



- $R_S = \rho / t$
- $V_H = 1.15\,\mathrm{mV}$
- $n_s = n \cdot t = 10^{-8} \frac{IB}{qV_{H,avg}}$
- $n = 1.1 \times 10^{17}\,\mathrm{cm}^{-3}$
- High *n* implies oxygen contamination

Hall Mobility Measurements



- $R_S = \rho / t$
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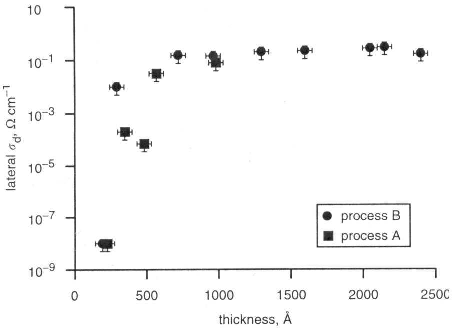
- $n_s = n \cdot t = 10^{-8} \frac{IB}{qV_{H,avg}}$
- $n = 1.1 \times 10^{17}\,\mathrm{cm}^{-3}$
- High n implies oxygen contamination
- $\mu_H = \frac{1}{qn_s R_S}$
- $\mu_H = 0.27\,\mathrm{cm}^2\ \mathrm{V}^{-1}\ \mathrm{s}^{-1}$
- This is higher than quoted a-Si:H value

Discussion

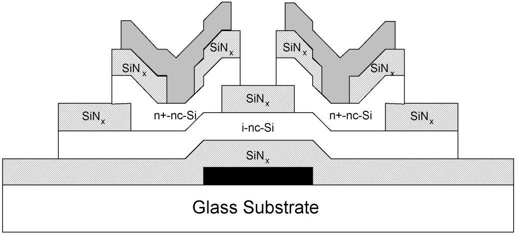


Conductivity of nc-Si p-layer deposited on textured TCO substrate by pulsed PECVD [Das, 2003].

- As seen in graph, a high crystallinity was expected at 50 nm thickness
- In this thesis, 50 nm films using the similar processing conditions are amorphous whereas 300 nm films are crystalline
- Therefore, incubation layer is large ⇒ possibly due to different substrate

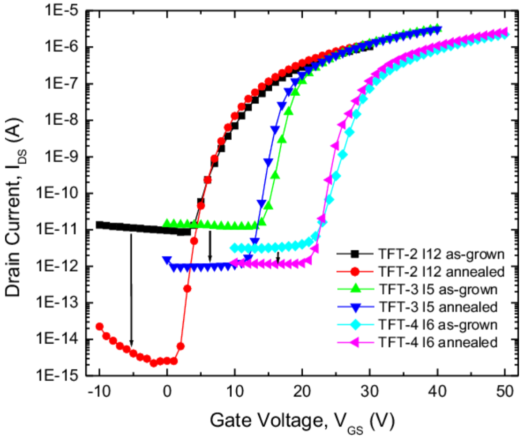
Outline

Bottom-Gate TFT Structure



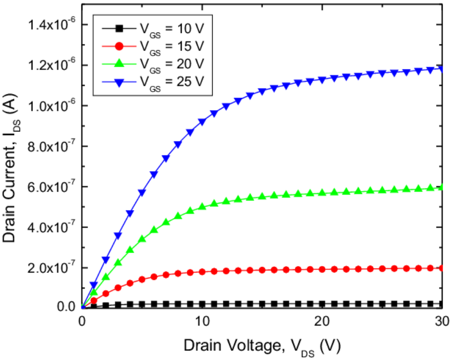
- Trilayer deposited at MVSystems, everything else at Waterloo
- All channel layers deposited at 150 °C
- Channel thickness: 50 nm, a-SiN$_x$: 250 nm
- Channel layer deposited according to the same parameters as for samples 50-1 to 50-4 and 300-1 to 300-4.

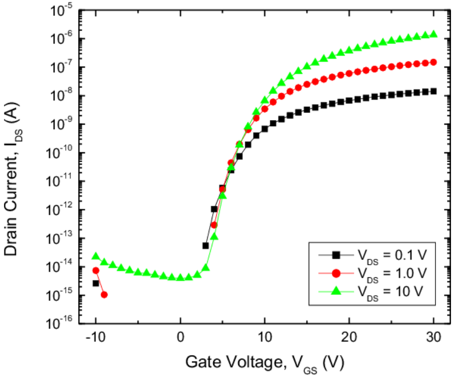
Annealing Effect



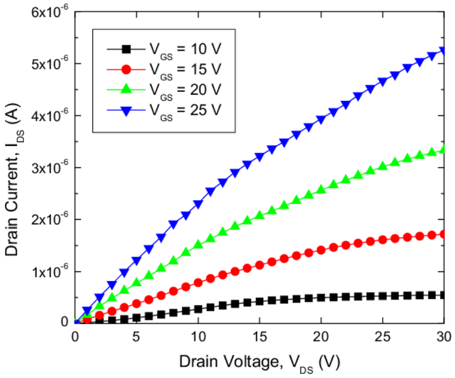
- Annealed at 150 °C for two hours in vacuum
- The subthreshold slope, S, and the off-current, I_{off}, are improved, I_{on} shows slight increase
- Improvement is due to annealing of bulk and interface defect states, and annealing of contacts

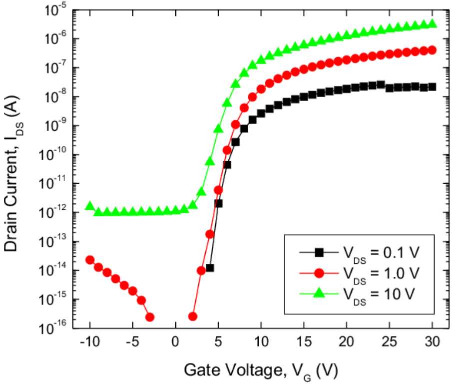
TFT Results for typical TFT-2 device



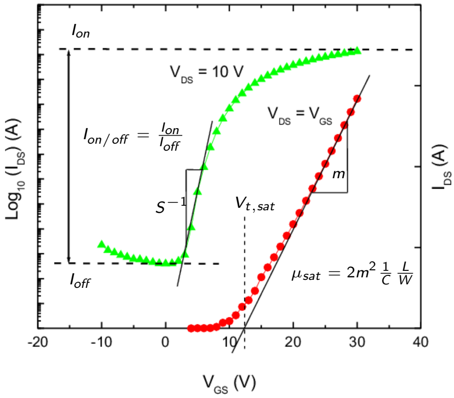


TFT Results for typical TFT-3 and TFT-4 device





Extraction



Extractions were performed using a simple equation:

$$I_{DS,lin} = \mu_{lin} C_i \frac{W}{L}(V_G - V_{t,lin}) \cdot V_{DS},$$

and

$$I_{DS,sat} = \frac{1}{2}\mu_{sat} C_i \frac{W}{L}(V_G - V_{t,sat})^2$$

Extracted Parameters with $V_{DS} = 0.1\,\mathrm{V}$ and $V_{DS} = V_{GS}$

TFT	$\mu_{lin}\left(\frac{\mathrm{cm}^2}{\mathrm{V{\cdot}s}}\right)$	$\mu_{sat}\left(\frac{\mathrm{cm}^2}{\mathrm{V{\cdot}s}}\right)$	$V_{t,lin}$ (V)	$V_{t,sat}$ (V)
TFT-2	0.02-0.10	0.12-0.17	9.9-12.4	11.6-13.6
TFT-3	0.23-0.27	0.34-0.38	9.6-11.3	7.5-9.6
TFT-4	0.28-0.30	0.34-0.46	11.8-13.0	7.3-9.5

- Mobility is very low in TFT-2 but TFT-3/4 mobility is similar to that of other low temperature a-Si:H TFTs
- Threshold voltage is high in all devices ⇒ may be due to poor materials (channel and/or dielectric)

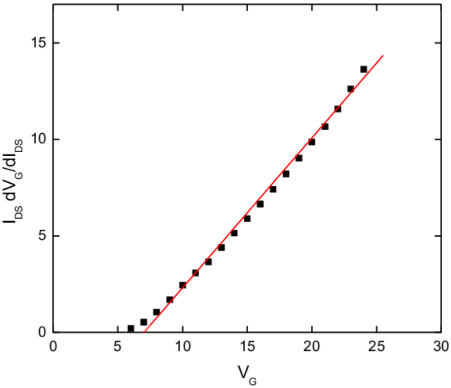
Extracted Parameters with $V_{DS} = 10\,\mathrm{V}$

TFT	$S\left(\frac{\mathrm{V}}{\mathrm{decade}}\right)$	$I_{on/off}$	$I_{off}(\mathrm{A})$
TFT-2	0.46-0.81	$> 10^7$	$< 10^{-14}$
TFT-3	0.76-0.95	$> 10^6$	$< 10^{-12}$
TFT-4	0.76-1.20	$> 10^6$	$\leq 10^{-12}$

- I_{off} is low and correspondingly, $I_{on/off}$ is high enough for LCD applications
- Sub-threshold slope, S, is acceptable compared to other low-temperature TFTs ($< 1\,\mathrm{V/decade}$)

Extraction of α and V_t for TFT-3

$$I_{DS,lin} = \mu_{eff}\zeta C_i^{\alpha-1}\frac{W}{L_{eff}}(V_{GS} - V_T - 0.5V_{DS})^{\alpha-1}(V_{DS} - R_{DS}I_{DS})$$



- $\alpha = 2.28$ and $V_T = 7.22\,\text{V}$
- α and V_T are high

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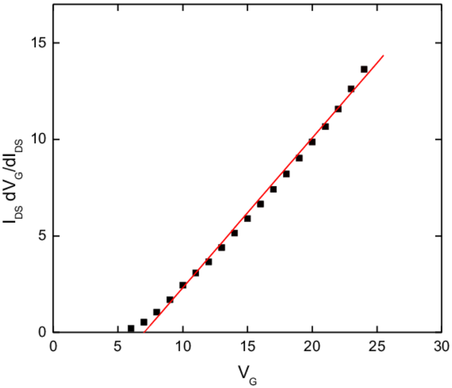

- $\alpha = 2.28$ and $V_T = 7.22\,\mathrm{V}$
- α and V_T are high
- $V_{nt} = 29.3\,\mathrm{mV}$
- V_{nt} (band tail slope) is high compared to high quality a-Si:H TFTs, indicating a high defect density of states

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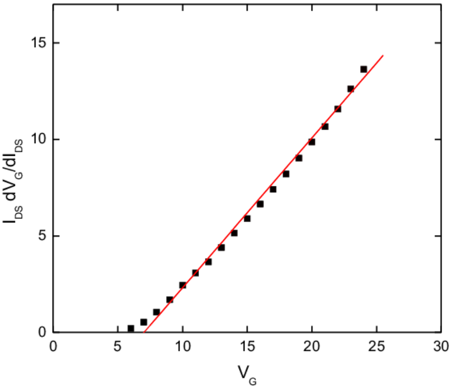

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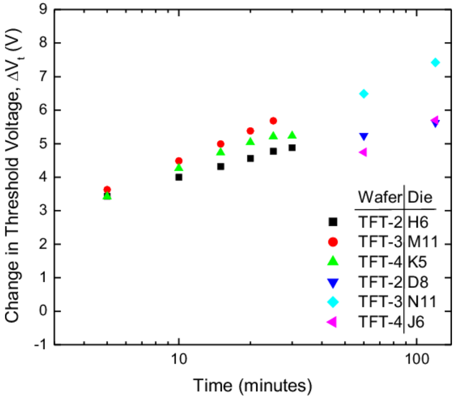
- α and V_T are high
- $V_{nt} = 29.3\,\mathrm{mV}$
- V_{nt} (band tail slope) is high compared to high quality a-Si:H TFTs, indicating a high defect density of states
- $\mu_{eff} = 0.23\,\mathrm{cm}^2\ \mathrm{V}^{-1}\ \mathrm{s}^{-1}$

TFT Stability



ΔV_T with 30 V bias stres

- The two main causes for threshold voltage shift are defect state creation at the interface and charge trapping in the SiN:H gate dielectric
- On short time scales the threshold voltage of these TFTs changed drastically ⇒ possibly due to charge trapping rather than defect creation

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Conclusion

- 50 nm films were amorphous, so incubation must be larger than expected
- 300 nm films deposited with hydrogen dilution showed high crystallinity
- Oxygen contamination is high in the crystalline samples, as seen from conductivity data and Hall measurement
- TFTs show reasonable performance compared to standard low-temperature TFTs, with good $I_{on/off}$, I_{off}, however, the layers must optimized to improve V_T, μ
- Gate bias metastability is high due to charge trapping in a-SiN$_x$:H dielectric

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- Thanks to OGS
- Most of all thanks to my fiancée Nasha and my family in Vancouver

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In *Proc. of 21st Int. Disp. Conf. and 8th Int. Disp. Workshops*, page 367. Soc. Info. Disp., 2001.