4-bit Transmission Gate Adder in 0.18µm CMOS

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Our Adder

- Conditional Carry-select (CCS) architecture using Transmission Gate (TG) Static CMOS
- Advantages:
  - Low-voltage, low-power operation possible
  - Scales relatively well to higher bit words
  - Small, compact layout due to TG gates
  - Can be scaled for improved performance

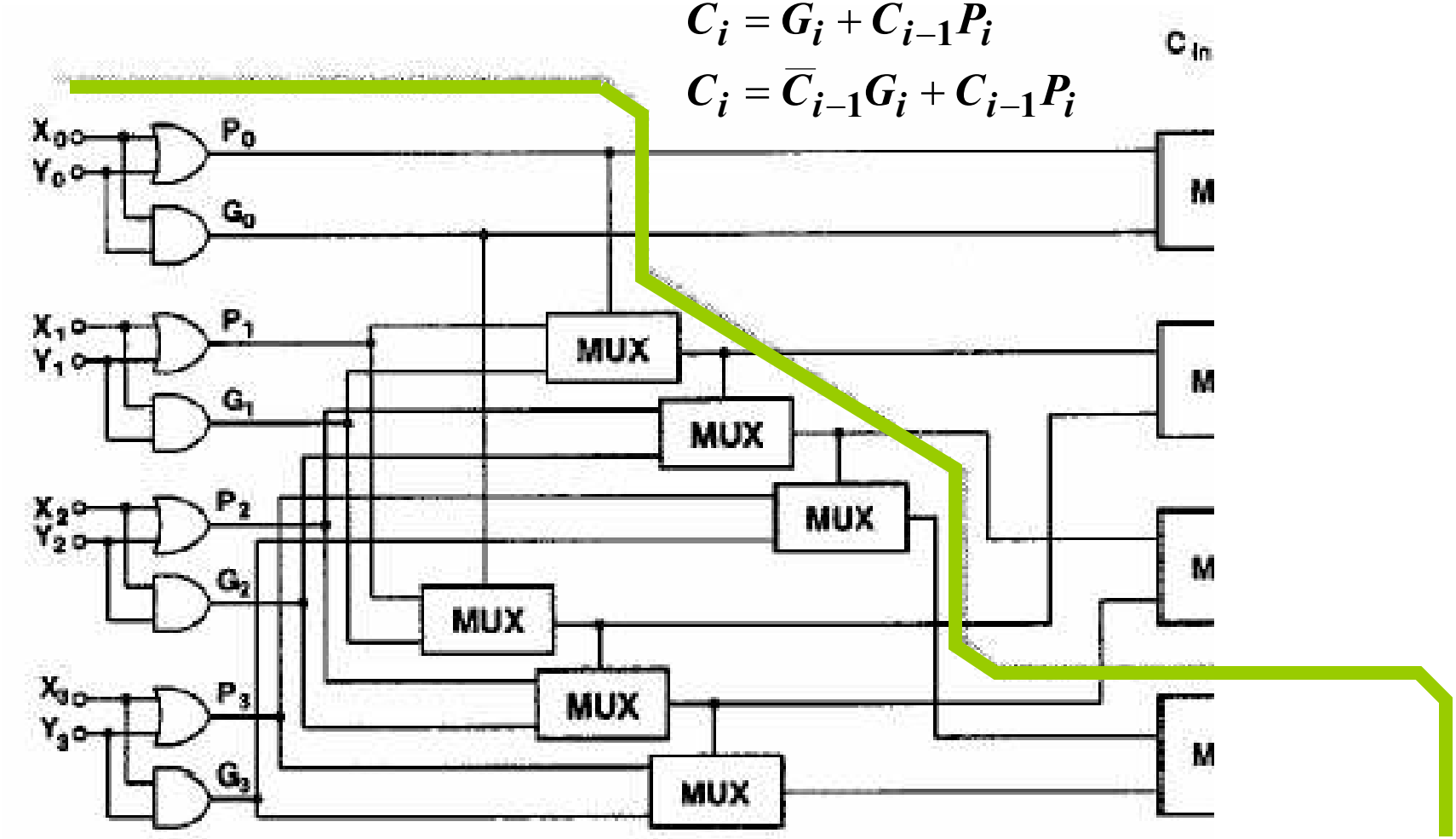
Current Status

- Completed schematics and sizing
- Layout: 80% finished assuming no major W/L changes

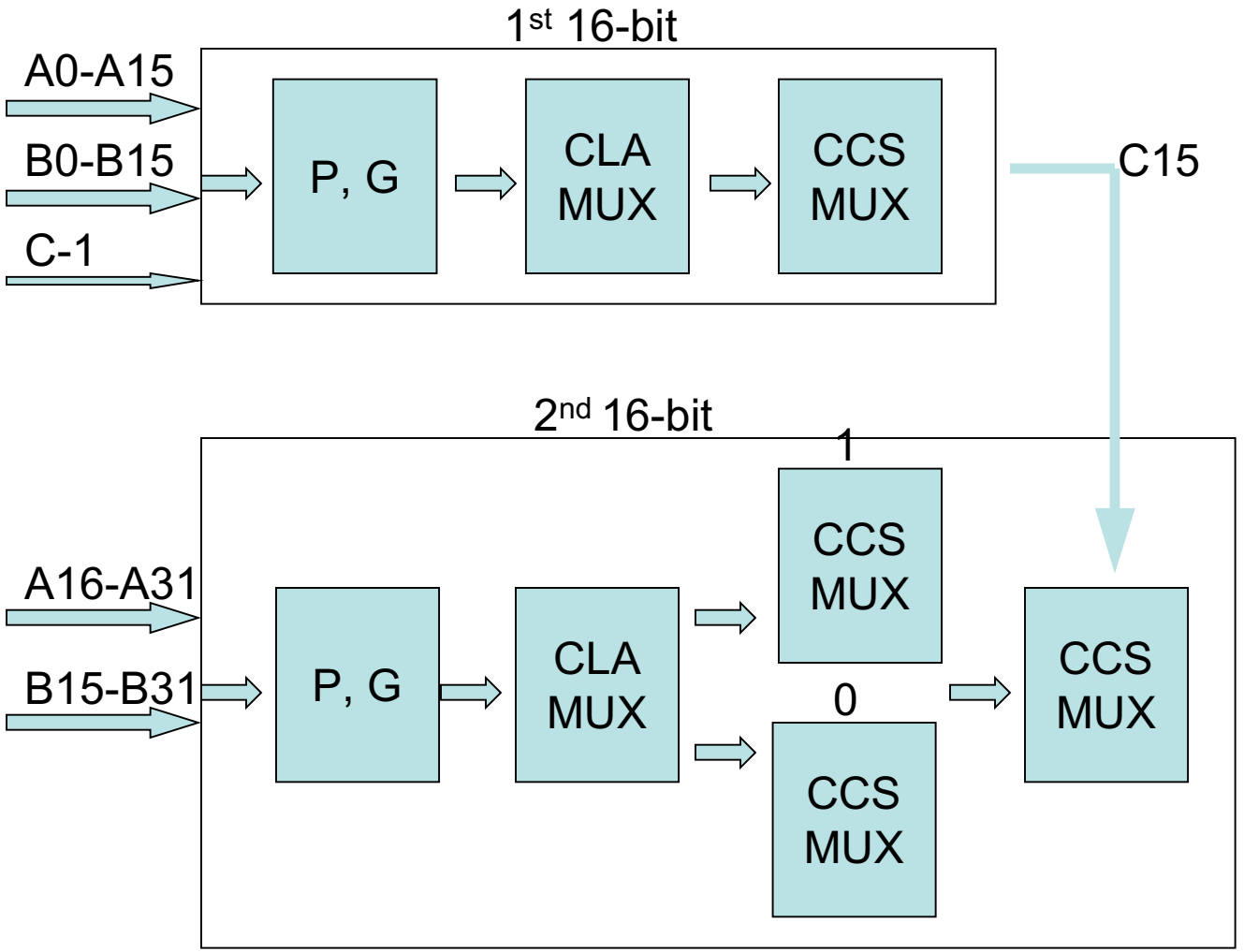
4-bit Block Diagram

$$C_i = G_i + C_{i-1}P_i$$

$$C_i = \overline{C}_{i-1}G_i + C_{i-1}P_i$$

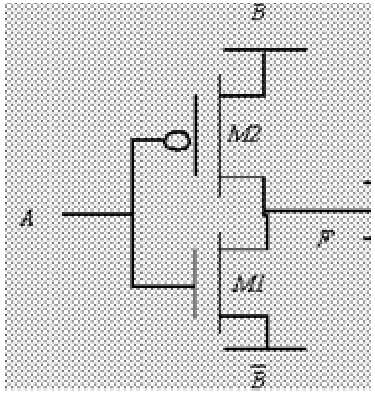


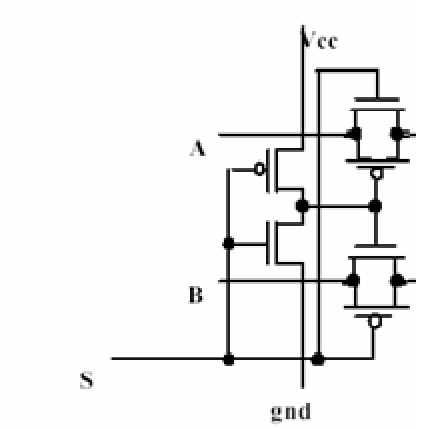
32-bit Architecture



Blocks

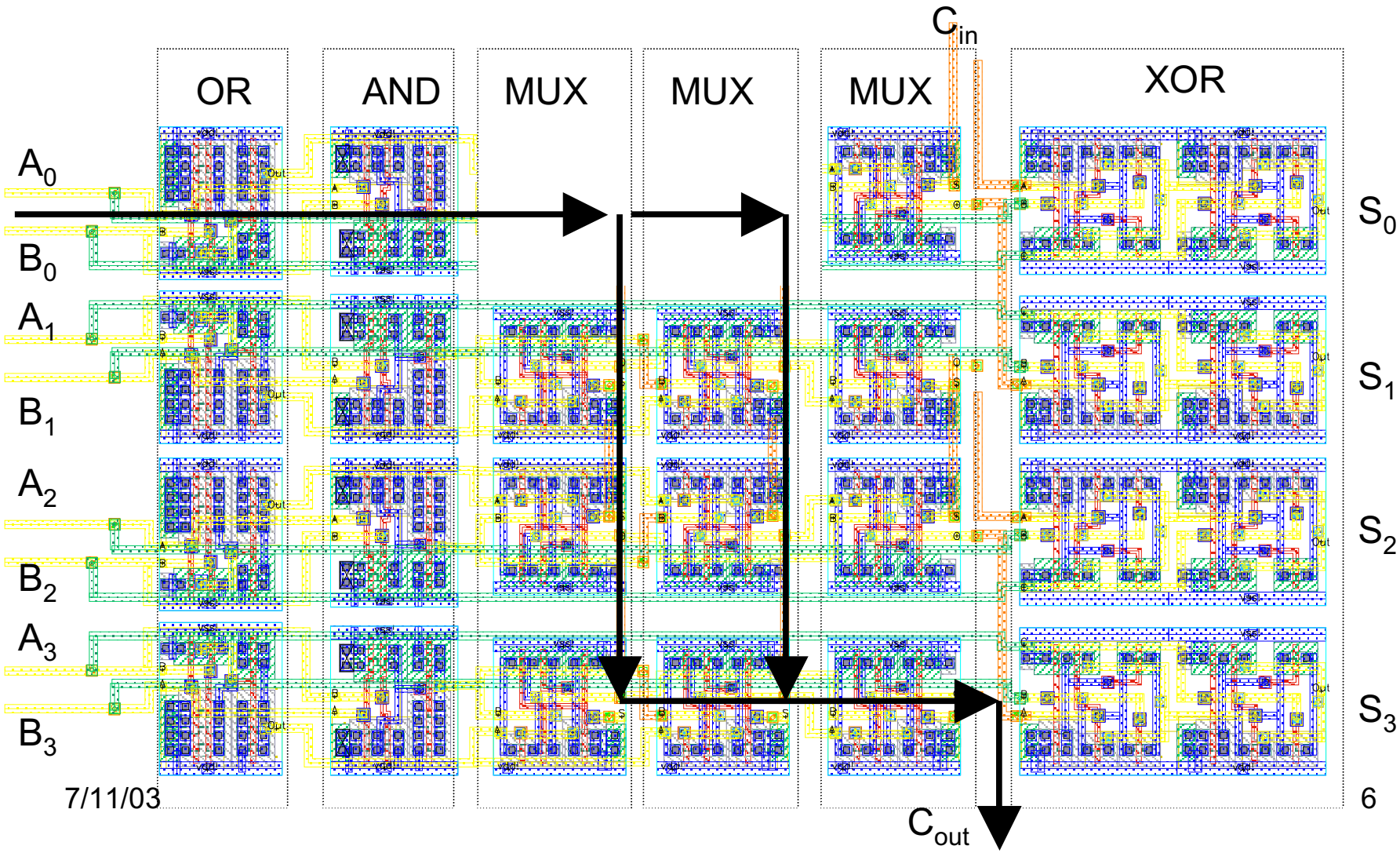
- 3-input TG XOR gate:
  (for sum generation)
- TG MUX
- AND (static CMOS)
- OR (static CMOS)





Layout

- TG MUX is the most important stage in critical path



Performance (or lack thereof)

Specification	*Value (4-bit block)*
Technology	0.18um
Power	155 µW (1.8V), 22 µW (0.8V)
Area	600 μm^2 - 700 μm^2
Transistors	144 (88 for standard CMOS, 56 for TG)
Delay (τ_d) at 1.8V	520 ps (4-bit), 1.4 ns (32-bit)
P×τ_d	568 × 10^{-14} J
Lowest Voltage	0.8V

Things to Do/Think About

- Using larger PMOS device in TG to improve rise time for 1s thus making rise/fall times symmetric.
- Need to finish routing between blocks for 4-bit module
- Need to simulate extracted layout, and test 32-bit, etc…